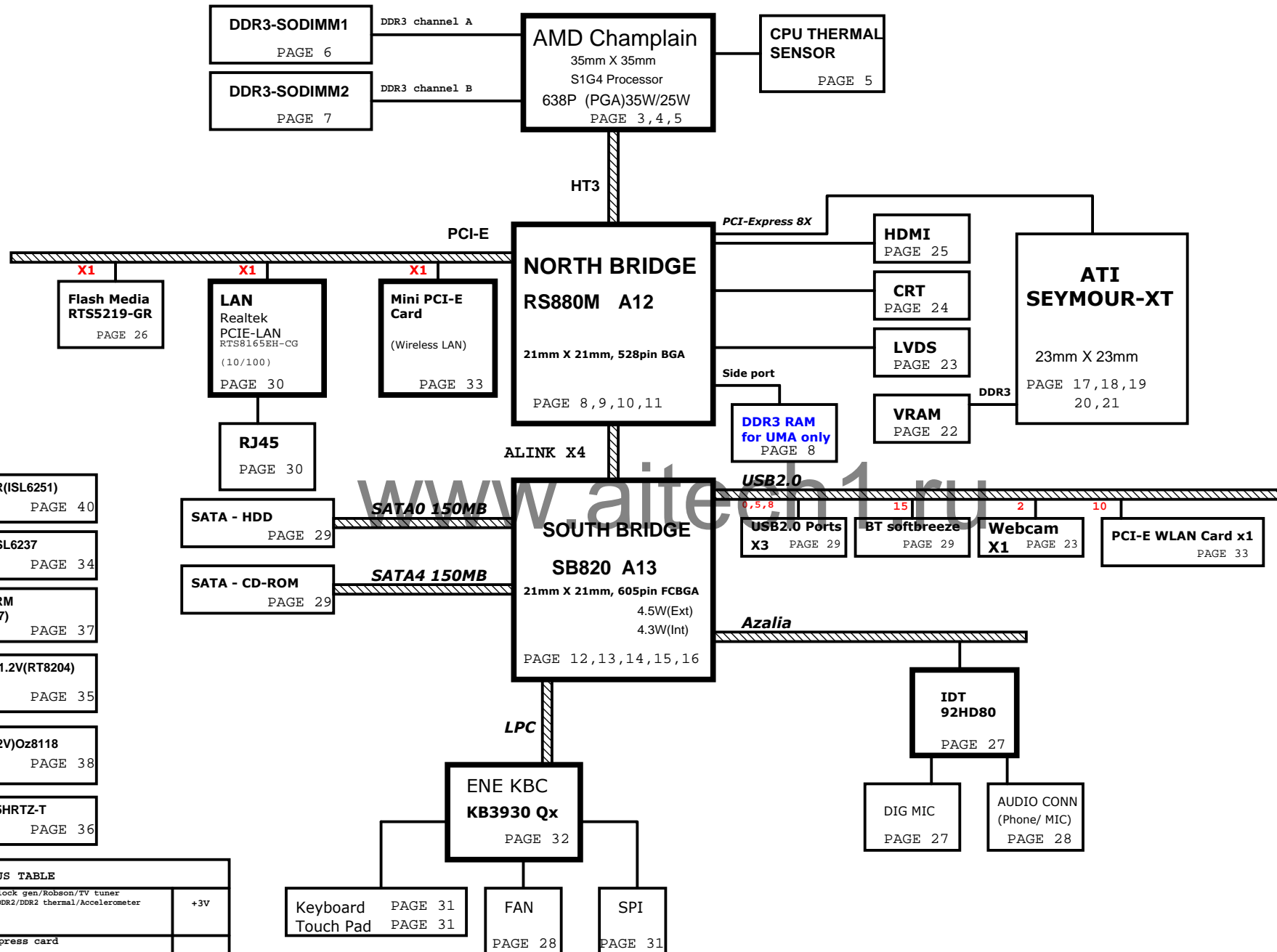


R22 SYSTEM DIAGRAM



01



SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

Use internal CLK GEN

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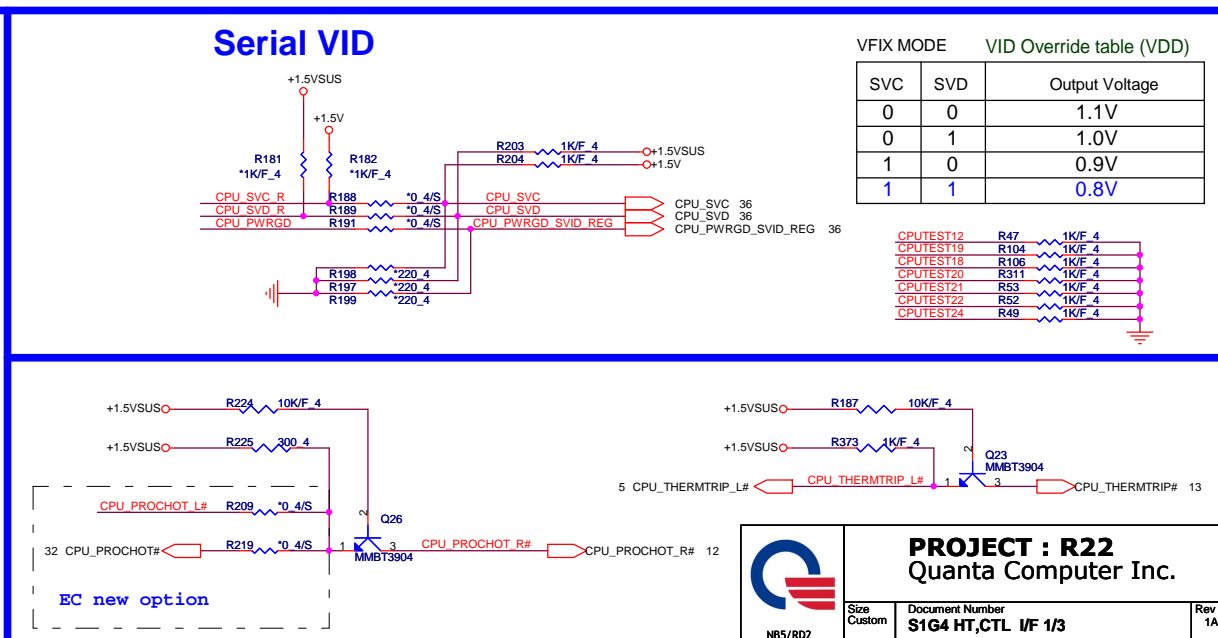
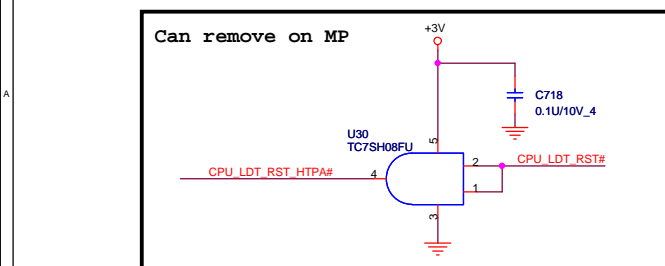
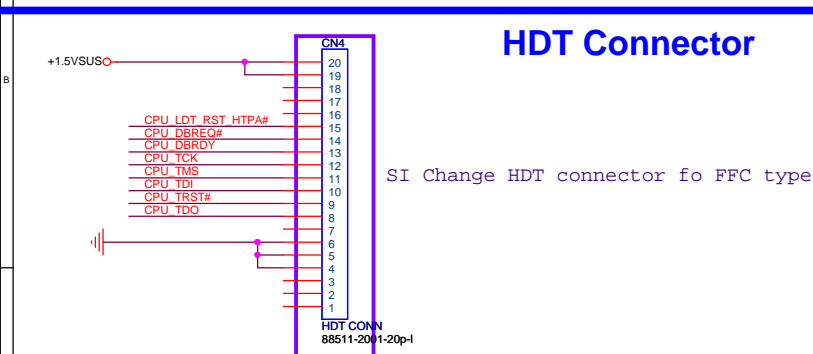
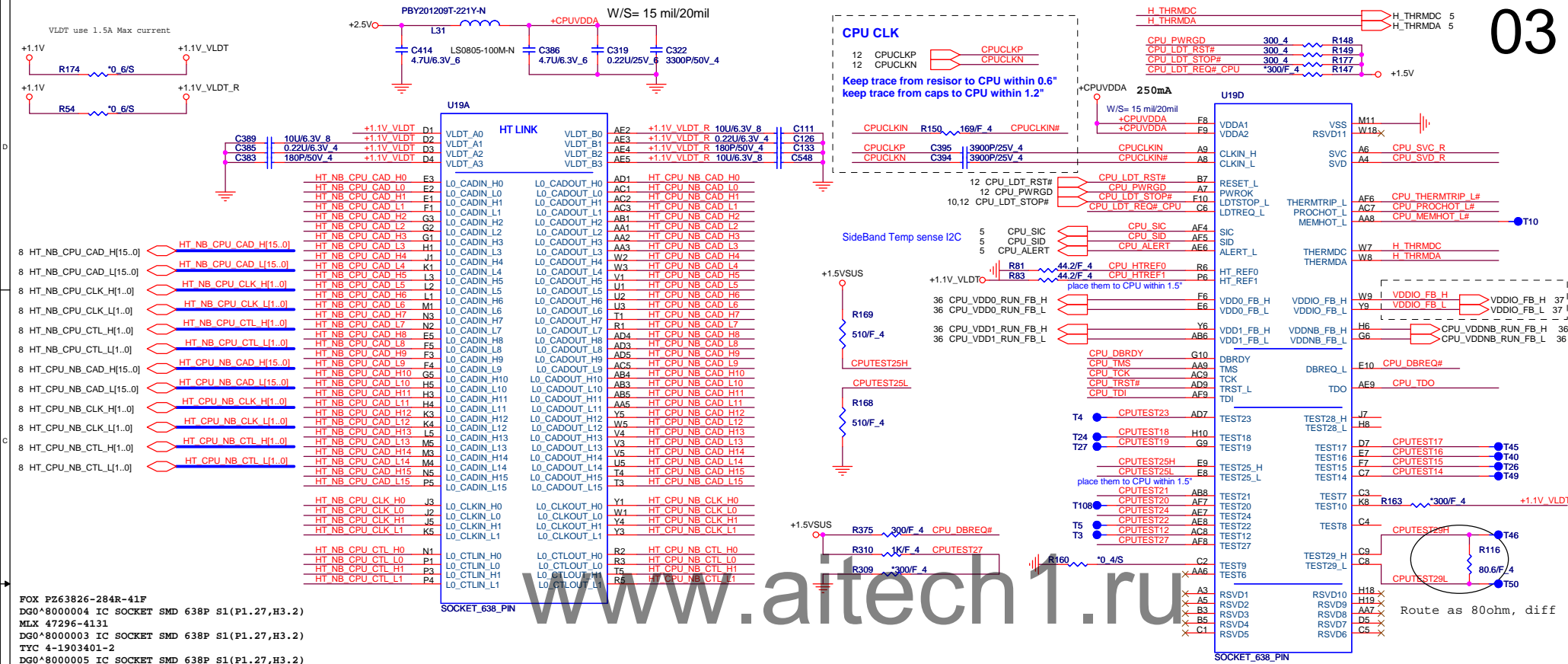


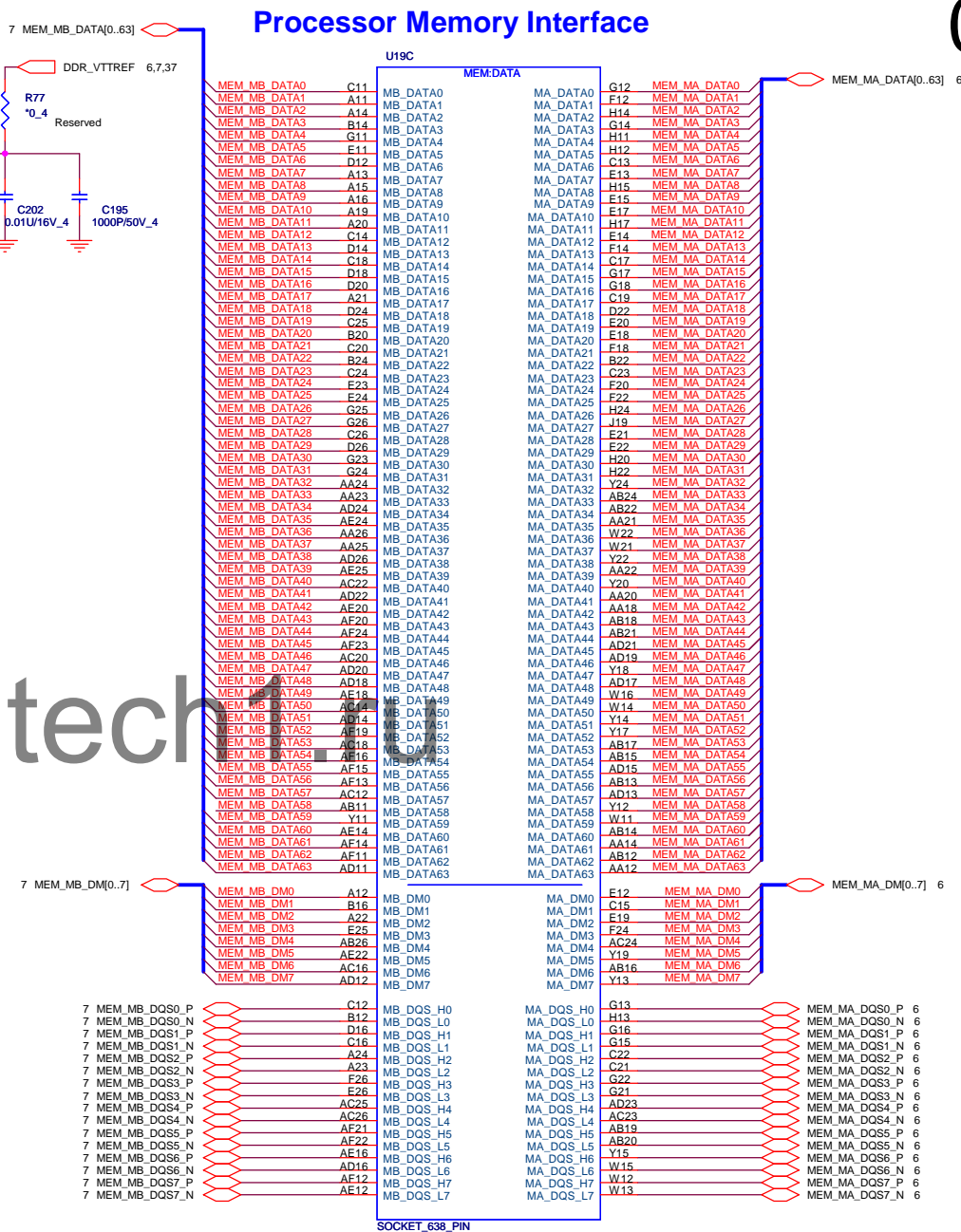
NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size
CustomDocument Number
Clock GeneratorRev
1A

Date: Wednesday, September 15, 2011 Sheet 2 of 43







Size Custom	Document Number DDR3 SODIMMS: A/B CHANNEL	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 6 of 43		

HT_CPU_NB_CAD_H[15..0] HT_CPU_NB_CAD_H[15..0] 3
 HT_CPU_NB_CAD_L[15..0] HT_CPU_NB_CAD_L[15..0] 3
 HT_CPU_NB_CLK_H[1..0] HT_CPU_NB_CLK_H[1..0] 3
 HT_CPU_NB_CLK_L[1..0] HT_CPU_NB_CLK_L[1..0] 3
 HT_CPU_NB_CTL_H[1..0] HT_CPU_NB_CTL_H[1..0] 3
 HT_CPU_NB_CTL_L[1..0] HT_CPU_NB_CTL_L[1..0] 3
 HT_NB_CPU_CAD_H[15..0] HT_NB_CPU_CAD_H[15..0] 3
 HT_NB_CPU_CAD_L[15..0] HT_NB_CPU_CAD_L[15..0] 3
 HT_NB_CPU_CLK_H[1..0] HT_NB_CPU_CLK_H[1..0] 3
 HT_NB_CPU_CLK_L[1..0] HT_NB_CPU_CLK_L[1..0] 3
 HT_NB_CPU_CTL_H[1..0] HT_NB_CPU_CTL_H[1..0] 3
 HT_NB_CPU_CTL_L[1..0] HT_NB_CPU_CTL_L[1..0] 3

HT_CPU_NB_CAD_H0 Y25 HT_RXCAD0P
 HT_CPU_NB_CAD_L0 Y24 HT_RXCAD0N
 HT_CPU_NB_CAD_H1 V22 HT_RXCAD1P
 HT_CPU_NB_CAD_L1 V23 HT_RXCAD1N
 HT_CPU_NB_CAD_H2 V25 HT_RXCAD2P
 HT_CPU_NB_CAD_L2 V24 HT_RXCAD2N
 HT_CPU_NB_CAD_H3 U24 HT_RXCAD3P
 HT_CPU_NB_CAD_L3 U25 HT_RXCAD3N
 HT_CPU_NB_CAD_H4 T25 HT_RXCAD4P
 HT_CPU_NB_CAD_L4 T24 HT_RXCAD4N
 HT_CPU_NB_CAD_H5 P23 HT_RXCAD5P
 HT_CPU_NB_CAD_L5 P25 HT_RXCAD5N
 HT_CPU_NB_CAD_H6 P24 HT_RXCAD6P
 HT_CPU_NB_CAD_L6 N24 HT_RXCAD6N
 HT_CPU_NB_CAD_H7 N25 HT_RXCAD7P
 HT_CPU_NB_CAD_L7 N25 HT_RXCAD7N

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CPU_NB_CAD_H8 AC24 HT_RXCAD8P
 HT_CPU_NB_CAD_L8 AC25 HT_RXCAD8N
 HT_CPU_NB_CAD_H9 AB25 HT_RXCAD9P
 HT_CPU_NB_CAD_L9 AB24 HT_RXCAD9N
 HT_CPU_NB_CAD_H10 AA24 HT_RXCAD10P
 HT_CPU_NB_CAD_L10 AA25 HT_RXCAD10N
 HT_CPU_NB_CAD_H11 Y23 HT_RXCAD11P
 HT_CPU_NB_CAD_L11 W21 HT_RXCAD11N
 HT_CPU_NB_CAD_H12 W21 HT_RXCAD12P
 HT_CPU_NB_CAD_L12 W20 HT_RXCAD12N
 HT_CPU_NB_CAD_H13 V21 HT_RXCAD13P
 HT_CPU_NB_CAD_L13 V20 HT_RXCAD13N
 HT_CPU_NB_CAD_H14 U20 HT_RXCAD14P
 HT_CPU_NB_CAD_L14 U21 HT_RXCAD14N
 HT_CPU_NB_CAD_H15 U19 HT_RXCAD15P
 HT_CPU_NB_CAD_L15 U18 HT_RXCAD15N

HT_TXCAD0P D24 HT_NB_CPU_CAD_H8
 HT_TXCAD0N D25 HT_NB_CPU_CAD_L8
 HT_TXCAD1P E24 HT_NB_CPU_CAD_H9
 HT_TXCAD1N E25 HT_NB_CPU_CAD_L9
 HT_TXCAD2P F24 HT_NB_CPU_CAD_H2
 HT_TXCAD2N F25 HT_NB_CPU_CAD_L2
 HT_TXCAD3P F22 HT_NB_CPU_CAD_H3
 HT_TXCAD3N F23 HT_NB_CPU_CAD_L3
 HT_TXCAD4P H22 HT_NB_CPU_CAD_H4
 HT_TXCAD4N H23 HT_NB_CPU_CAD_L4
 HT_TXCAD5P J25 HT_NB_CPU_CAD_H5
 HT_TXCAD5N J24 HT_NB_CPU_CAD_L5
 HT_TXCAD6P K25 HT_NB_CPU_CAD_H6
 HT_TXCAD6N K24 HT_NB_CPU_CAD_L6
 HT_TXCAD7P K23 HT_NB_CPU_CAD_H7
 HT_TXCAD7N K22 HT_NB_CPU_CAD_L7

signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

SPM_VREF1 M9 VREFCA
 SPM_VREF2 H2 VREFDQ
 SPM_A0 N4 A0 DQ0
 SPM_A1 P6 A1 DQ1
 SPM_A2 P4 A2 DQ2
 SPM_A3 N3 A3 DQ3
 SPM_A4 P9 A4 DQ4
 SPM_A5 P3 A5 DQ5
 SPM_A6 R9 A6 DQ6
 SPM_A7 R3 A7 DQ7
 SPM_A8 T9 A8 DQ8
 SPM_A9 R4 A9 DQ9
 SPM_A10 L8 A10/AP DQ10
 SPM_A11 R8 A11 DQ11
 SPM_A12 N8 A12/BC DQ12
 SPM_A13 T4 A13 DQ13
 T8 A14 DQ14
 M8 A15 DQ15

E4 SPM_DQ0
 F8 SPM_DQ1
 F3 SPM_DQ2
 E9 SPM_DQ3
 H4 SPM_DQ4
 G3 SPM_DQ5
 H8 SPM_DQ6
 D8 SPM_DQ13
 C4 SPM_DQ8
 C9 SPM_DQ10
 C3 SPM_DQ12
 A8 SPM_DQ15
 A3 SPM_DQ11
 B9 SPM_DQ14
 A4 SPM_DQ9

SPM_BA0 M3 BA0 VDD#B3
 SPM_BA1 N9 BA1 VDD#D10
 SPM_BA2 M4 BA2 VDD#G8
 SPM_CLKP J8 CK VDD#K3
 SPM_CLKN K8 CK VDD#N2
 SPM_CKE K10 CK VDD#N10
 SPM_ODT K2 ODT VDD#A2
 SPM_CS# L3 CS VDD#A9
 SPM_RAS# J4 RAS VDD#C2
 SPM_CAS# K4 CAS VDD#C10
 SPM_WE# L4 WE VDD#D3
 SPM_DQSOP F4 DQSL VDD#F2
 SPM_DQS1P C8 DQSU VDD#H10

B3 +1.5V_MEM_VDDQ
 D10 +1.5V_MEM_VDDQ
 G8 +1.5V_MEM_VDDQ
 K3 +1.5V_MEM_VDDQ
 N2 +1.5V_MEM_VDDQ
 R10 +1.5V_MEM_VDDQ
 A2 +1.5V_MEM_VDDQ
 A9 +1.5V_MEM_VDDQ
 C2 +1.5V_MEM_VDDQ
 C10 +1.5V_MEM_VDDQ
 D3 +1.5V_MEM_VDDQ
 E10 +1.5V_MEM_VDDQ
 F2 +1.5V_MEM_VDDQ
 F3 +1.5V_MEM_VDDQ
 H10 +1.5V_MEM_VDDQ

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4 DQSL VSS#T2
 SPM_DQS1N B8 DQSU VSS#T10

A10 VSS#A10
 B4 VSS#B4
 E2 VSS#E2
 F9 VSS#F9
 J3 VSS#J3
 J9 VSS#J9
 M2 VSS#M2
 M10 VSS#M10
 P2 VSS#P2
 P10 VSS#P10
 T2 VSS#T2
 T10 VSS#T10

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4 DQSL VSS#T2
 SPM_DQS1N B8 DQSU VSS#T10

A10 VSS#A10
 B4 VSS#B4
 E2 VSS#E2
 F9 VSS#F9
 J3 VSS#J3
 J9 VSS#J9
 M2 VSS#M2
 M10 VSS#M10
 P2 VSS#P2
 P10 VSS#P10
 T2 VSS#T2
 T10 VSS#T10

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4 DQSL VSS#T2
 SPM_DQS1N B8 DQSU VSS#T10

A10 VSS#A10
 B4 VSS#B4
 E2 VSS#E2
 F9 VSS#F9
 J3 VSS#J3
 J9 VSS#J9
 M2 VSS#M2
 M10 VSS#M10
 P2 VSS#P2
 P10 VSS#P10
 T2 VSS#T2
 T10 VSS#T10

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4 DQSL VSS#T2
 SPM_DQS1N B8 DQSU VSS#T10

A10 VSS#A10
 B4 VSS#B4
 E2 VSS#E2
 F9 VSS#F9
 J3 VSS#J3
 J9 VSS#J9
 M2 VSS#M2
 M10 VSS#M10
 P2 VSS#P2
 P10 VSS#P10
 T2 VSS#T2
 T10 VSS#T10

HT_RXCALP C23 HT_RXCALN A24
 HT_RXCALP C23 HT_RXCALN A24

HT_TXCALP R359 HT_TXCALN R359
 HT_TXCALP R359 HT_TXCALN R359

HT_CPU_NB_CLK_H0 T22 HT_RXCLK0P
 HT_CPU_NB_CLK_L0 T23 HT_RXCLK0N
 HT_CPU_NB_CLK_H1 AB23 HT_RXCLK1P
 HT_CPU_NB_CLK_L1 AA22 HT_RXCLK1N

HT_TXCLK0P H24 HT_NB_CPU_CLK_H0
 HT_TXCLK0N H25 HT_NB_CPU_CLK_L0
 HT_TXCLK1P L21 HT_NB_CPU_CLK_H1
 HT_TXCLK1N L20 HT_NB_CPU_CLK_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

HT_CPU_NB_CTL_H0 M22 HT_RXCTL0P
 HT_CPU_NB_CTL_L0 M23 HT_RXCTL0N
 HT_CPU_NB_CTL_H1 R21 HT_RXCTL1P
 HT_CPU_NB_CTL_L1 R20 HT_RXCTL1N

HT_TXCTL0P M24 HT_NB_CPU_CTL_H0
 HT_TXCTL0N M25 HT_NB_CPU_CTL_L0
 HT_TXCTL1P P19 HT_NB_CPU_CTL_H1
 HT_TXCTL1N P18 HT_NB_CPU_CTL_L1

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This block is for UMA only, DIS can remove all component

SPM_A0 AB12 MEM_A0(NC)
 SPM_A1 AE16 MEM_A1(NC)
 SPM_A2 V11 MEM_A2(NC)
 SPM_A3 AE15 MEM_A3(NC)
 SPM_A4 AB16 MEM_A4(NC)
 SPM_A5 AB16 MEM_A5(NC)
 SPM_A6 AB14 MEM_A6(NC)
 SPM_A7 AD14 MEM_A7(NC)
 SPM_A8 AD15 MEM_A8(NC)
 SPM_A9 AC16 MEM_A9(NC)
 SPM_A10 AE13 MEM_A10(NC)
 SPM_A11 AC14 MEM_A11(NC)
 SPM_A12 Y14 MEM_A12(NC)
 SPM_A13 Y14 MEM_A13(NC)

MEM_DQ0(DVO_VSYNC(NC)) AA18 SPM_DQ0
 MEM_DQ1(DVO_HSYNC(NC)) AA20 SPM_DQ1
 MEM_DQ2(DVO_DE(NC)) AA19 SPM_DQ2
 MEM_DQ3(DVO_D0(NC)) Y17 SPM_DQ3
 MEM_DQ4(NC) AA17 SPM_DQ4
 MEM_DQ5(DVO_D1(NC)) Y15 SPM_DQ5
 MEM_DQ6(DVO_D2(NC)) AC20 SPM_DQ6
 MEM_DQ7(DVO_D3(NC)) AD19 SPM_DQ7
 MEM_DQ8(DVO_D4(NC)) AE22 SPM_DQ8
 MEM_DQ9(DVO_D5(NC)) AC18 SPM_DQ9
 MEM_DQ10(DVO_D6(NC)) AB20 SPM_DQ10
 MEM_DQ11(DVO_D7(NC)) AD22 SPM_DQ11
 MEM_DQ12(NC) AC22 SPM_DQ12
 MEM_DQ13(DVO_D8(NC)) AD21 SPM_DQ13
 MEM_DQ14(DVO_D9(NC)) Y17 SPM_DQ14
 MEM_DQ15(DVO_D10(NC)) W18 SPM_DQ15
 MEM_DQ16(DVO_D11(NC)) AD20 SPM_DQ16
 MEM_DQ17(DVO_D12(NC)) AE21 SPM_DQ17
 MEM_DQ18(DVO_D13(NC)) W17 SPM_DQ18
 MEM_DQ19(DVO_D14(NC)) AE19 SPM_DQ19

SPM_BA0 AD16 MEM_BA0(NC)
 SPM_BA1 AE17 MEM_BA1(NC)
 SPM_BA2 AD17 MEM_BA2(NC)
 SPM_RAS# W12 MEM_RASb(NC)
 SPM_CAS# Y12 MEM_CASb(NC)
 SPM_WE# AD18 MEM_WEb(NC)
 SPM_CS# AB13 MEM_CSb(NC)
 SPM_CKE AB18 MEM_CKE(NC)
 SPM_ODT Y14 MEM_ODT(NC)

MEM_DQS0P(DVO_IDCKP(NC)) Y17 SPM_DQS0P
 MEM_DQS1P(DVO_IDCKP(NC)) W18 SPM_DQS1P
 MEM_DQS2P(DVO_IDCKP(NC)) AD20 SPM_DQS2P
 MEM_DQS3P(DVO_IDCKP(NC)) AE21 SPM_DQS3P
 MEM_DQS4P(DVO_IDCKP(NC)) W17 SPM_DQS4P
 MEM_DQS5P(DVO_IDCKP(NC)) AE19 SPM_DQS5P
 MEM_DQS6P(DVO_IDCKP(NC)) Y17 SPM_DQS6P
 MEM_DQS7P(DVO_IDCKP(NC)) W18 SPM_DQS7P
 MEM_DQS8P(DVO_IDCKP(NC)) AD20 SPM_DQS8P
 MEM_DQS9P(DVO_IDCKP(NC)) AE21 SPM_DQS9P
 MEM_DQS10P(DVO_IDCKP(NC)) W17 SPM_DQS10P
 MEM_DQS11P(DVO_IDCKP(NC)) AE19 SPM_DQS11P
 MEM_DQS12P(DVO_IDCKP(NC)) Y17 SPM_DQS12P
 MEM_DQS13P(DVO_IDCKP(NC)) W18 SPM_DQS13P
 MEM_DQS14P(DVO_IDCKP(NC)) AD20 SPM_DQS14P
 MEM_DQS15P(DVO_IDCKP(NC)) AE21 SPM_DQS15P

SPM_CLKP V15 MEM_CLKP(NC)
 SPM_CLKN W14 MEM_CLKN(NC)
 SPM_COMP# AE12 MEM_COMP#(NC)
 SPM_COMPN AD12 MEM_COMPN(NC)

MEM_DQ0(DVO_VSYNC(NC)) AA18 SPM_DQ0
 MEM_DQ1(DVO_HSYNC(NC)) AA20 SPM_DQ1
 MEM_DQ2(DVO_DE(NC)) AA19 SPM_DQ2
 MEM_DQ3(DVO_D0(NC)) Y17 SPM_DQ3
 MEM_DQ4(NC) AA17 SPM_DQ4
 MEM_DQ5(DVO_D1(NC)) Y15 SPM_DQ5
 MEM_DQ6(DVO_D2(NC)) AC20 SPM_DQ6
 MEM_DQ7(DVO_D3(NC)) AD19 SPM_DQ7
 MEM_DQ8(DVO_D4(NC)) AE22 SPM_DQ8
 MEM_DQ9(DVO_D5(NC)) AC18 SPM_DQ9
 MEM_DQ10(DVO_D6(NC)) AB20 SPM_DQ10
 MEM_DQ11(DVO_D7(NC)) AD22 SPM_DQ11
 MEM_DQ12(NC) AC22 SPM_DQ12
 MEM_DQ13(DVO_D8(NC)) AD21 SPM_DQ13
 MEM_DQ14(DVO_D9(NC)) Y17 SPM_DQ14
 MEM_DQ15(DVO_D10(NC)) W18 SPM_DQ15
 MEM_DQ16(DVO_D11(NC)) AD20 SPM_DQ16
 MEM_DQ17(DVO_D12(NC)) AE21 SPM_DQ17
 MEM_DQ18(DVO_D13(NC)) W17 SPM_DQ18
 MEM_DQ19(DVO_D14(NC)) AE19 SPM_DQ19

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4 DQSL VSS#T2
 SPM_DQS1N B8 DQSU VSS#T10

MEM_DQS0P(DVO_IDCKP(NC)) Y17 SPM_DQS0P
 MEM_DQS1P(DVO_IDCKP(NC)) W18 SPM_DQS1P
 MEM_DQS2P(DVO_IDCKP(NC)) AD20 SPM_DQS2P
 MEM_DQS3P(DVO_IDCKP(NC)) AE21 SPM_DQS3P
 MEM_DQS4P(DVO_IDCKP(NC)) W17 SPM_DQS4P
 MEM_DQS5P(DVO_IDCKP(NC)) AE19 SPM_DQS5P
 MEM_DQS6P(DVO_IDCKP(NC)) Y17 SPM_DQS6P
 MEM_DQS7P(DVO_IDCKP(NC)) W18 SPM_DQS7P
 MEM_DQS8P(DVO_IDCKP(NC)) AD20 SPM_DQS8P
 MEM_DQS9P(DVO_IDCKP(NC)) AE21 SPM_DQS9P
 MEM_DQS10P(DVO_IDCKP(NC)) W17 SPM_DQS10P
 MEM_DQS11P(DVO_IDCKP(NC)) AE19 SPM_DQS11P
 MEM_DQS12P(DVO_IDCKP(NC)) Y17 SPM_DQS12P
 MEM_DQS13P(DVO_IDCKP(NC)) W18 SPM_DQS13P
 MEM_DQS14P(DVO_IDCKP(NC)) AD20 SPM_DQS14P
 MEM_DQS15P(DVO_IDCKP(NC)) AE21 SPM_DQS15P

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
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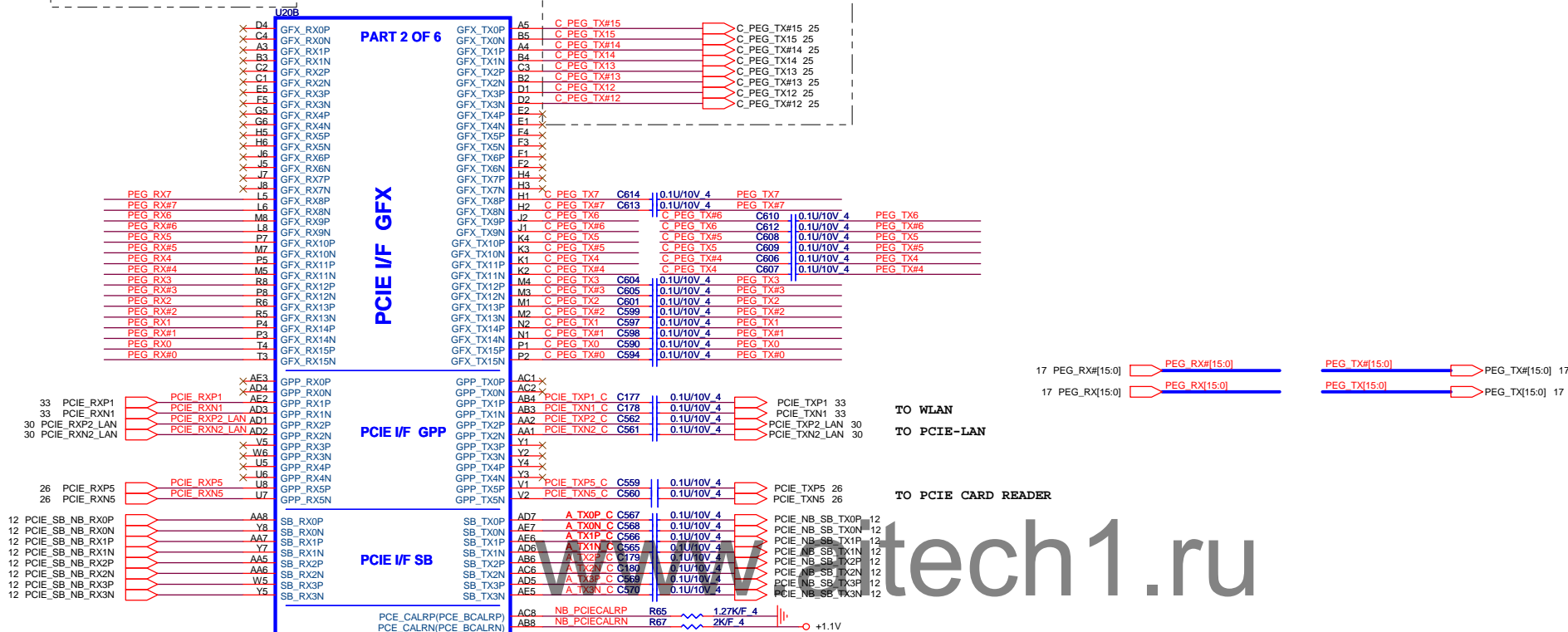
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 MEM_DQS3P(DVO_IDCKP(NC)) AE21 SPM_DQS3P
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 MEM_DQS6P(DVO_IDCKP(NC)) Y17 SPM_DQS6P
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 MEM_DQS10P(DVO_IDCKP(NC)) W17 SPM_DQS10P
 MEM_DQS11P(DVO_IDCKP(NC)) AE19 SPM_DQS11P
 MEM_DQS12P(DVO_IDCKP(NC)) Y17 SPM_DQS12P
 MEM_DQS13P(DVO_IDCKP(NC)) W18 SPM_DQS13P
 MEM_DQS14P(DVO_IDCKP(NC)) AD20 SPM_DQS14P
 MEM_DQS15P(DVO_IDCKP(NC)) AE21 SPM_DQS15P

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4 DQSL VSS#T2
 SPM_DQS1N B8 DQSU VSS#T10

MEM_DQS0P(DVO_IDCKP(NC)) Y17 SPM_DQS0P
 MEM_DQS1P(DVO_IDCKP(NC)) W18 SPM_DQS1P
 MEM_DQS2P(DVO_IDCKP(NC)) AD20 SPM_DQS2P
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 MEM_DQS5P(DVO_IDCKP(NC)) AE19 SPM_DQS5P
 MEM_DQS6P(DVO_IDCKP(NC)) Y17 SPM_DQS6P
 MEM_DQS7P(DVO_IDCKP(NC)) W18 SPM_DQS7P
 MEM_DQS8P(DVO_IDCKP(NC)) AD20 SPM_DQS8P
 MEM_DQS9P(DVO_IDCKP(NC)) AE21 SPM_DQS9P
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 MEM_DQS13P(DVO_IDCKP(NC)) W18 SPM_DQS13P
 MEM_DQS14P(DVO_IDCKP(NC)) AD20 SPM_DQS14P
 MEM_DQS15P(DVO_IDCKP(NC)) AE21 SPM_DQS15P

SPM_DM0 E8 DML VSS#A10
 SPM_DM1 D4 DMU VSS#B4
 SPM_DQS0N G4 DQSL VSS#E2
 SPM_DQS1N B8 DQSU VSS#F9
 SPM_DQS0N G4 DQSL VSS#J3
 SPM_DQS1N B8 DQSU VSS#J9
 SPM_DQS0N G4 DQSL VSS#M2
 SPM_DQS1N B8 DQSU VSS#M10
 SPM_DQS0N G4 DQSL VSS#P2
 SPM_DQS1N B8 DQSU VSS#P10
 SPM_DQS0N G4

To HDMI CONN



RS880

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

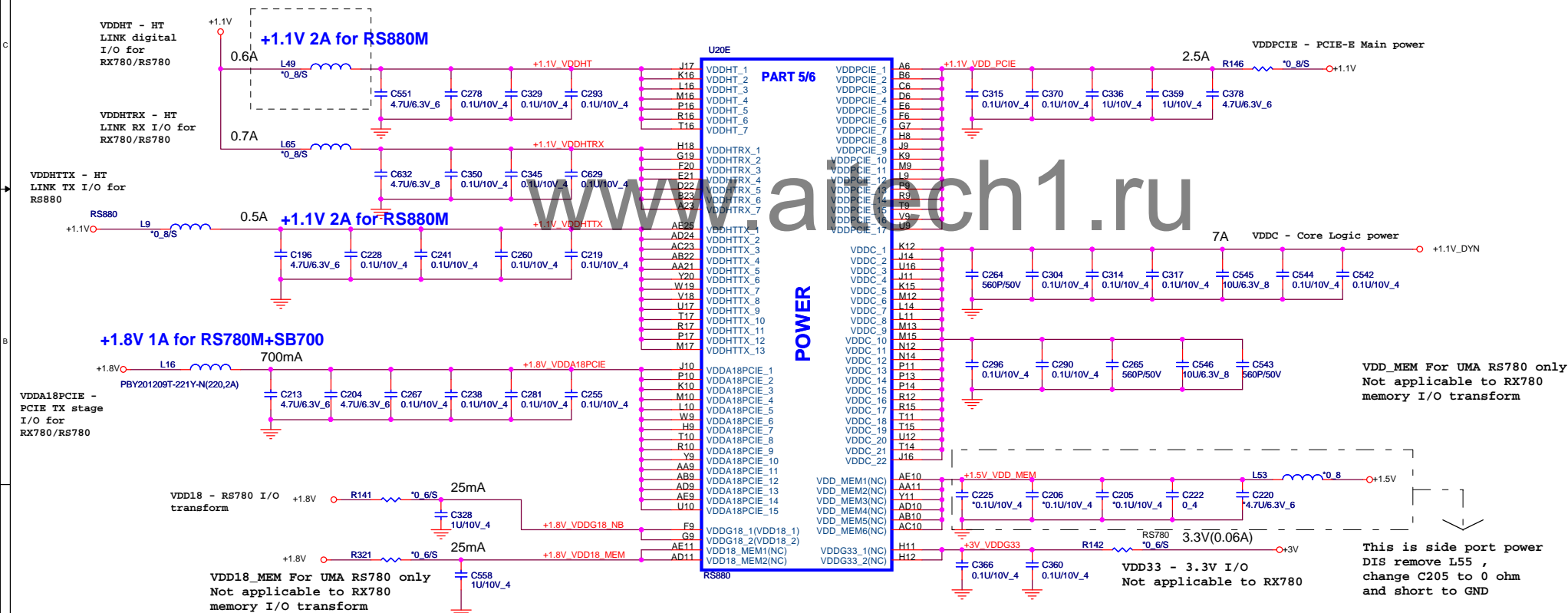
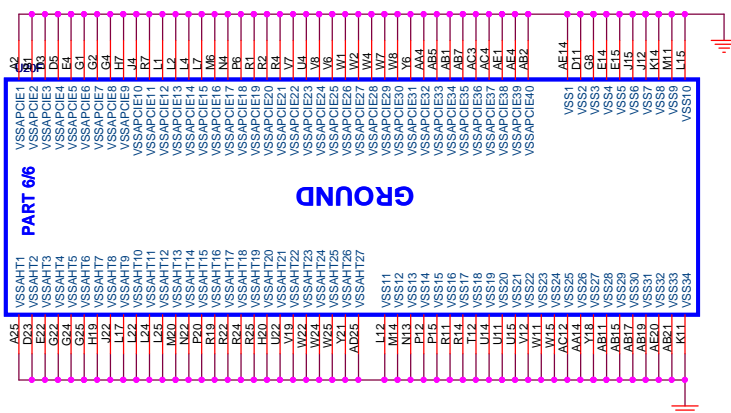


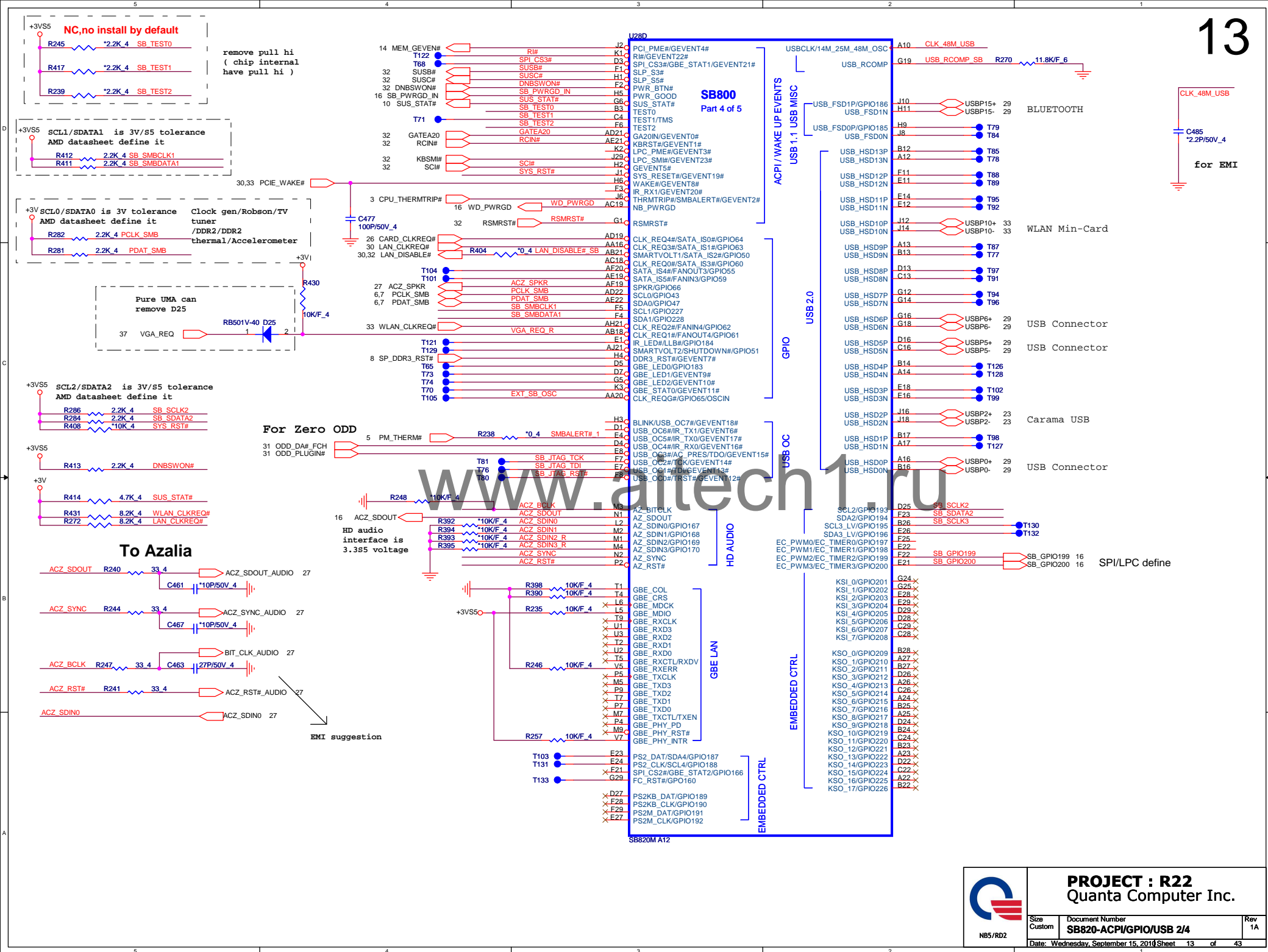


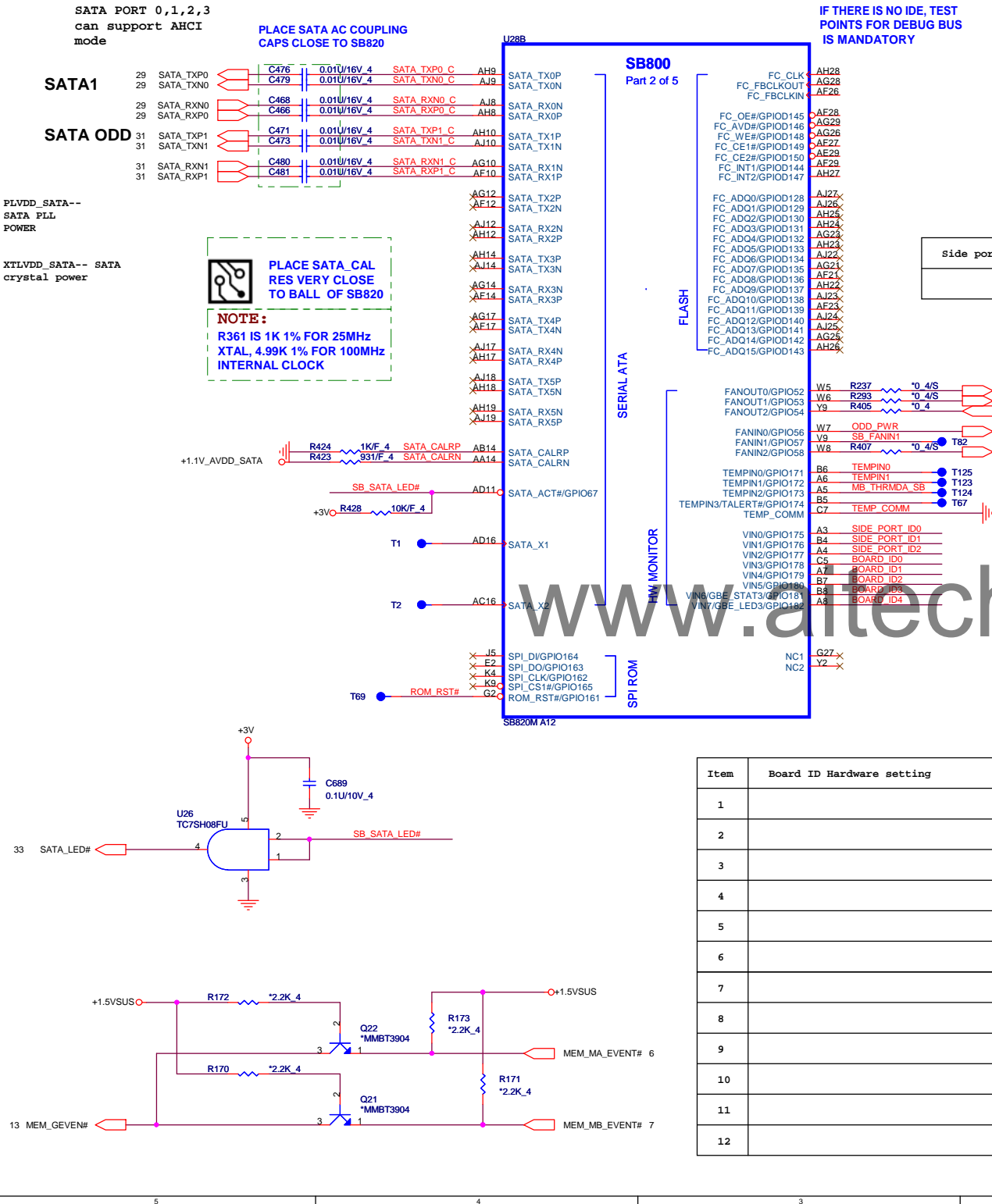
VDDL18 - LVDS or DVI/HDMI digital not applicable to RS880

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PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLT18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL1833	NC



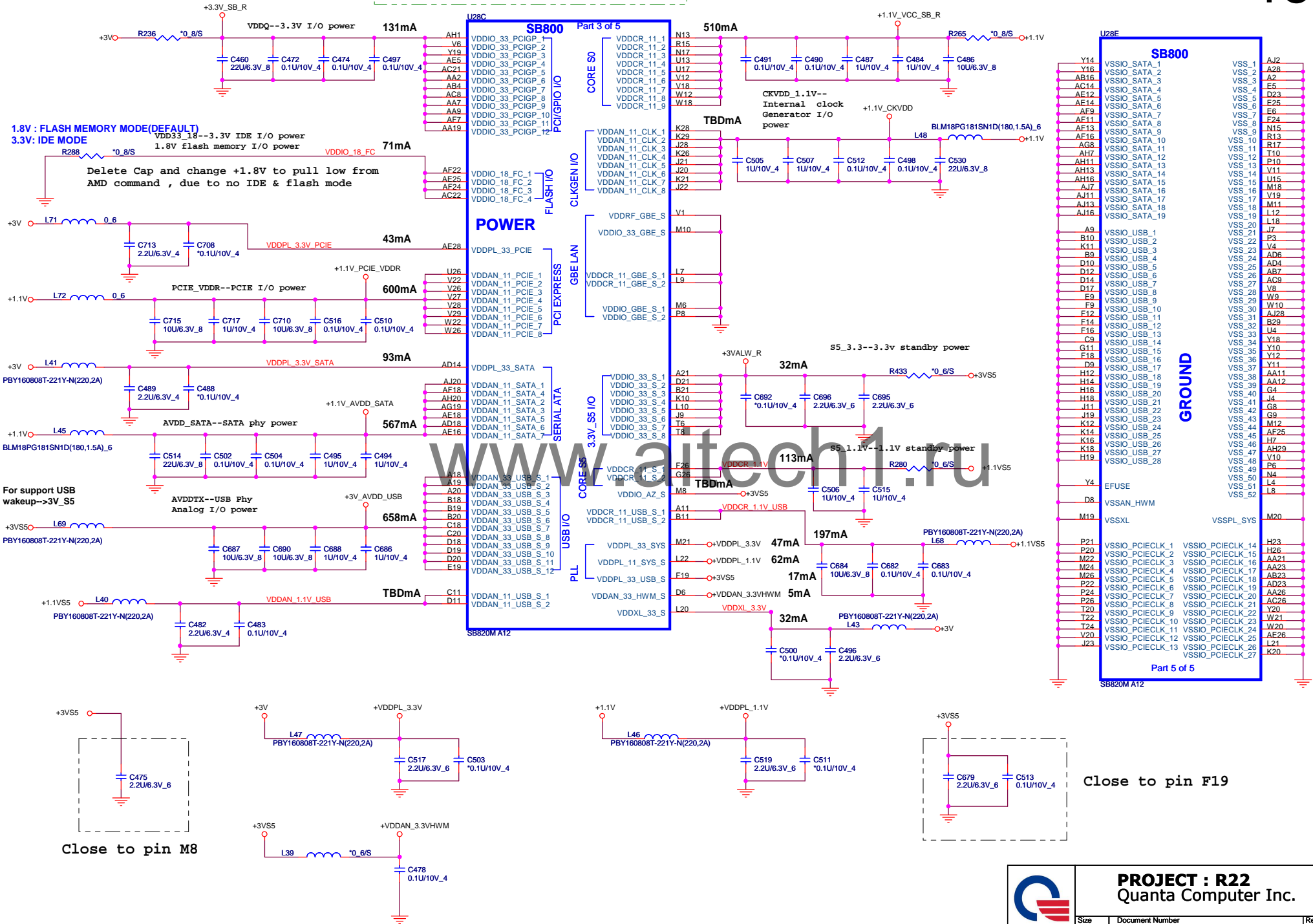






PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

15

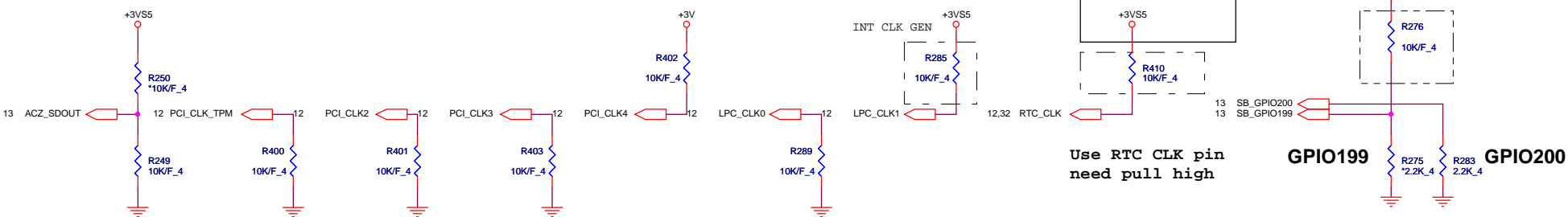


PROJECT : R22
Quanta Computer Inc.

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

REQUIRED STRAPS

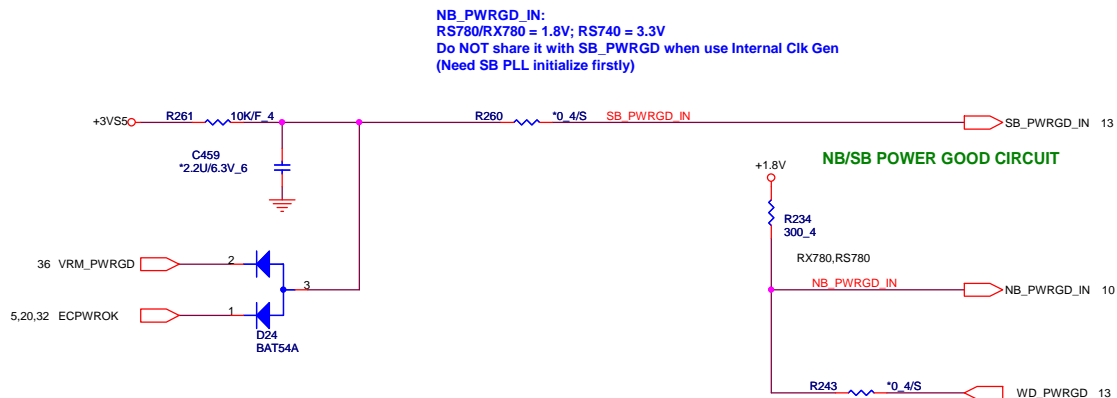


REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



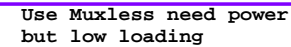
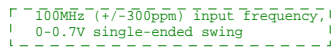
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5



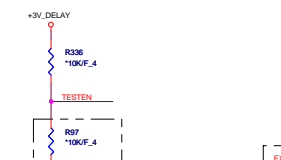
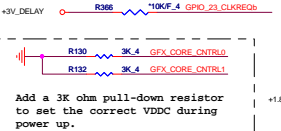
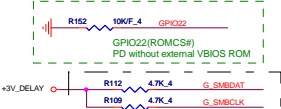
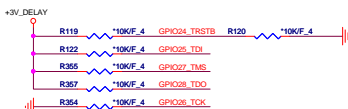
PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number SB820-STRAPS	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 16 of 43		

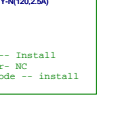
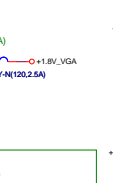
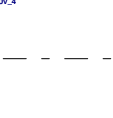
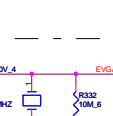
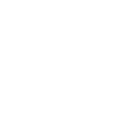
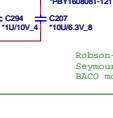
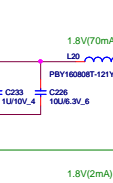
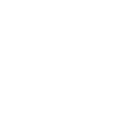
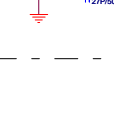
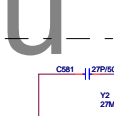
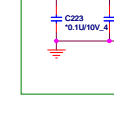
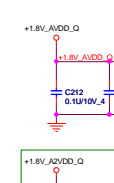
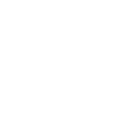
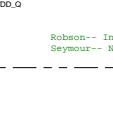
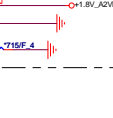
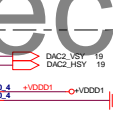
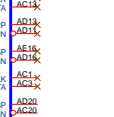
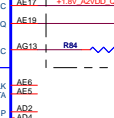
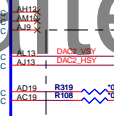
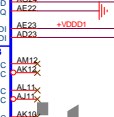
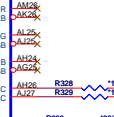
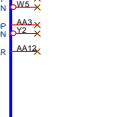
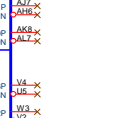
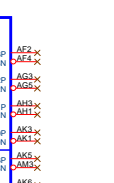
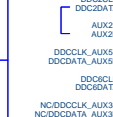
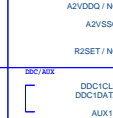
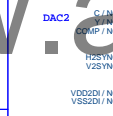
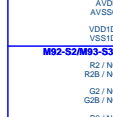
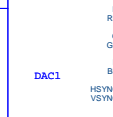
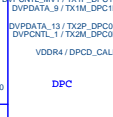
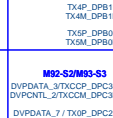
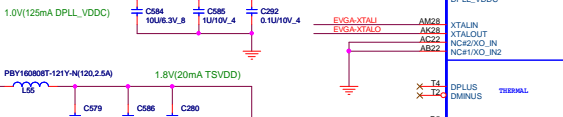
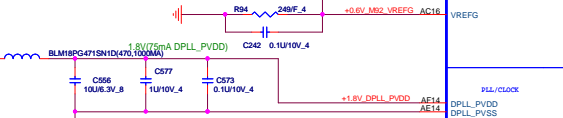
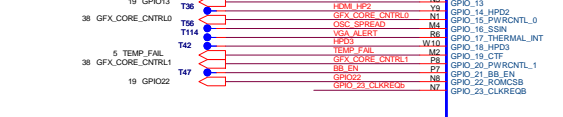
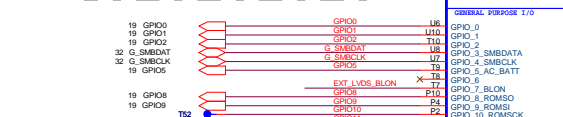
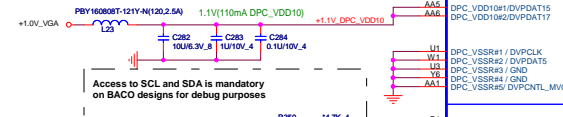
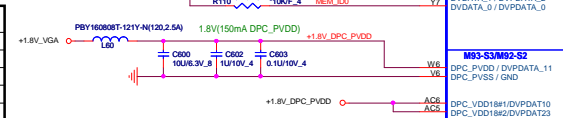
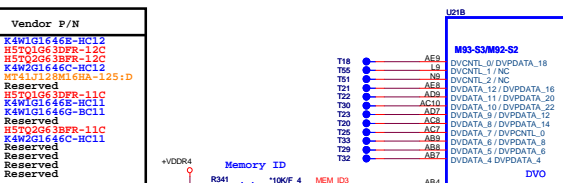


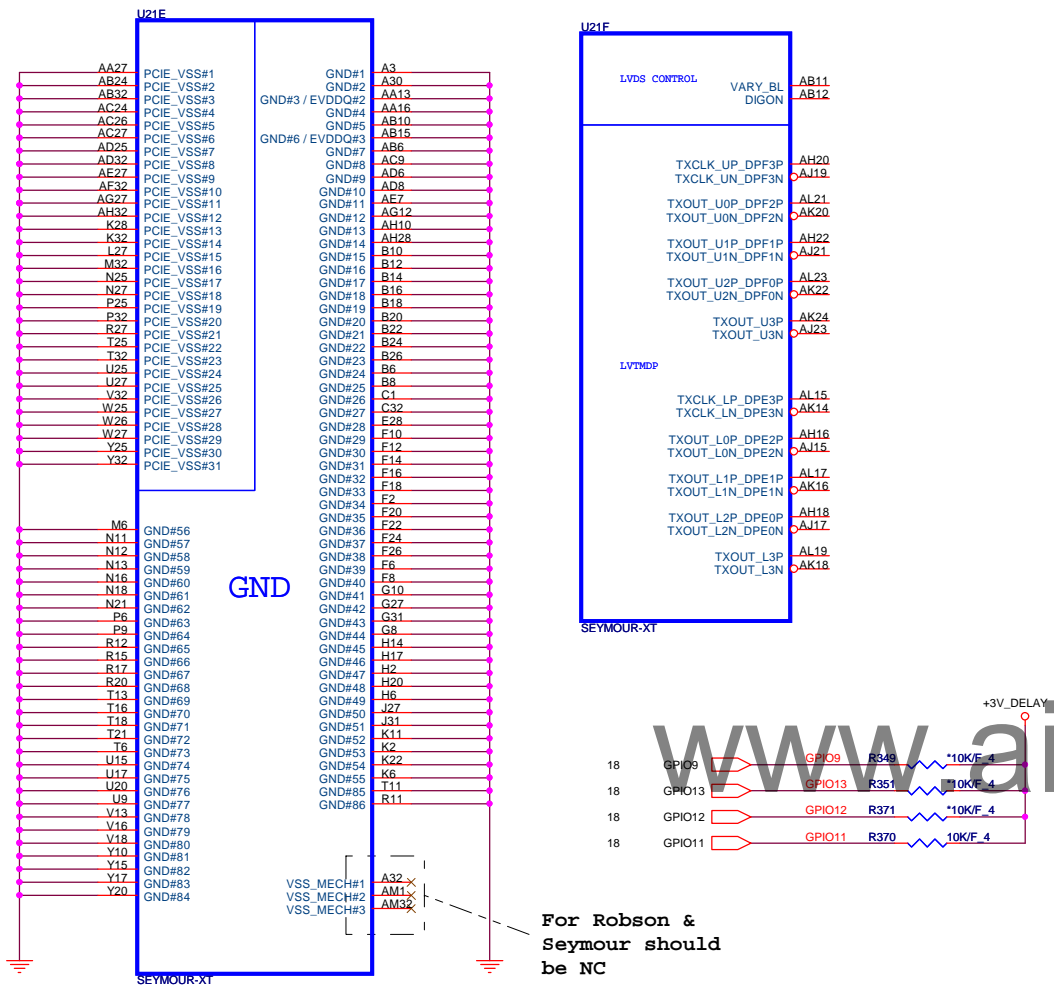
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0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-BC12
0100	Micro on	128*16-800MHZ	MT93J1250ML6DA-1251D
0110	Hynix- Vega die	64*16-900MHZ	Reserved
0111	Samsung- E die	64*16-900MHZ	H5TQ1G63DFR-11C
1000	Samsung- C die	64*16-900MHZ	K4W1G1646E-BC11
1001	Samsung- G die	64*16-900MHZ	Reserved
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-BC11
1100	Reserved		Reserved
1101	Reserved		Reserved
1110	Reserved		Reserved
1111	Reserved		Reserved

MEM_ID[3:0]	31 Level BOM	H/W setting
0000	TBD	TBD
0001	TBD	TBD
0010	TBD	TBD
0011	TBD	TBD
0100	TBD	TBD



If no contact this pin to LVDS need pull low

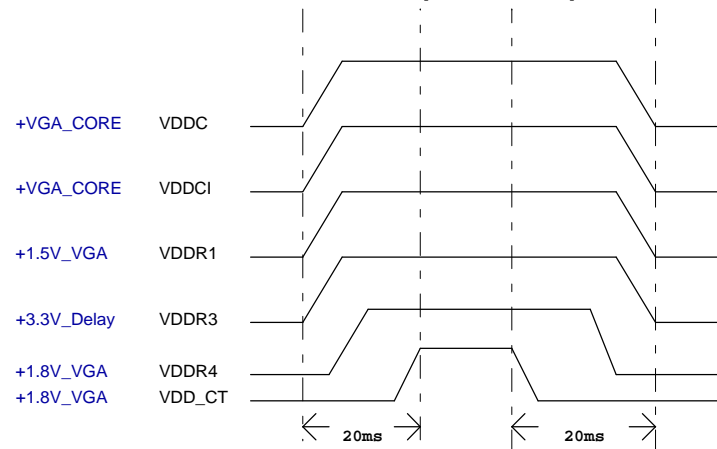




CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE	
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	
RSVD	GPIO2	RESERVED	0	
RSVD	GPIO8	RESERVED	0	
BIF_VGA_DIS	GPIO9	VGA ENABLED	0	
RSVD	GPIO21	RESERVED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0	
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1	
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0	
RSVD	H2SYNC	RESERVED	0	
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0	
AUD[0]	VSYS	SEE DATABOOK FOR DETAIL	0	
RSVD	GENERICC	RESERVED	0	

NOTE1: AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.				
GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2

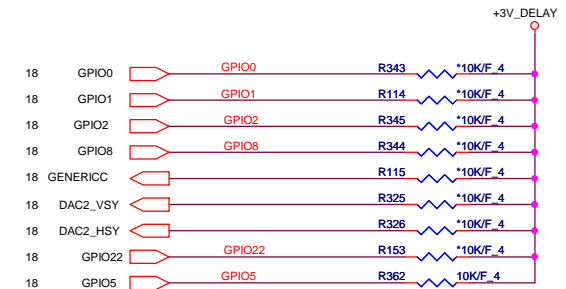
Power Up/Down Sequence



Memory Aperture size

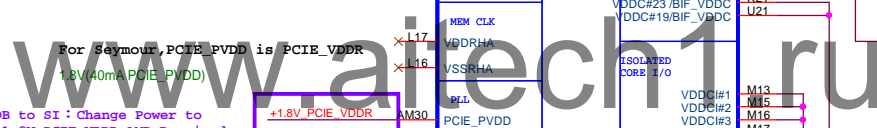
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

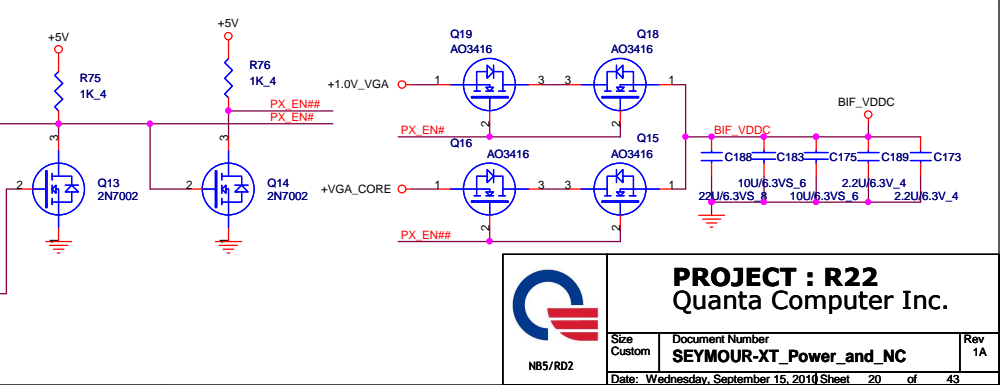


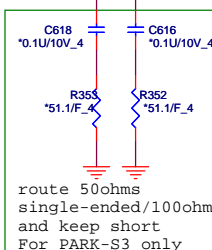
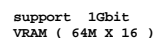
PROJECT : R22
Quantas Computer Inc.

Size Custom	Document Number SEYMOUR-XT GND / LVDS/ Straps	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 19	of 43



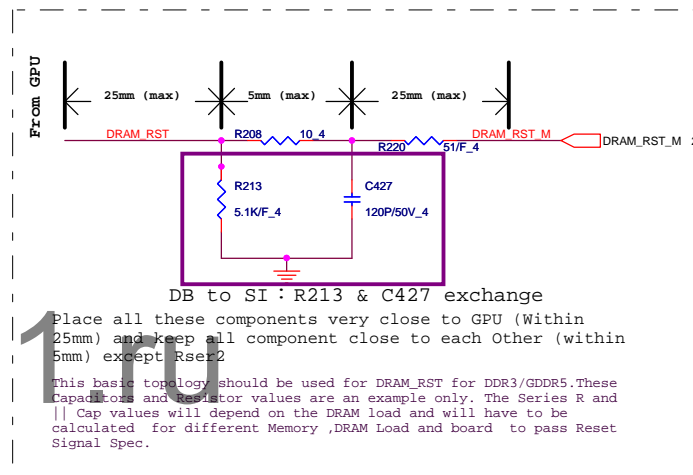
SI:change BACO circuit for AMD recommand





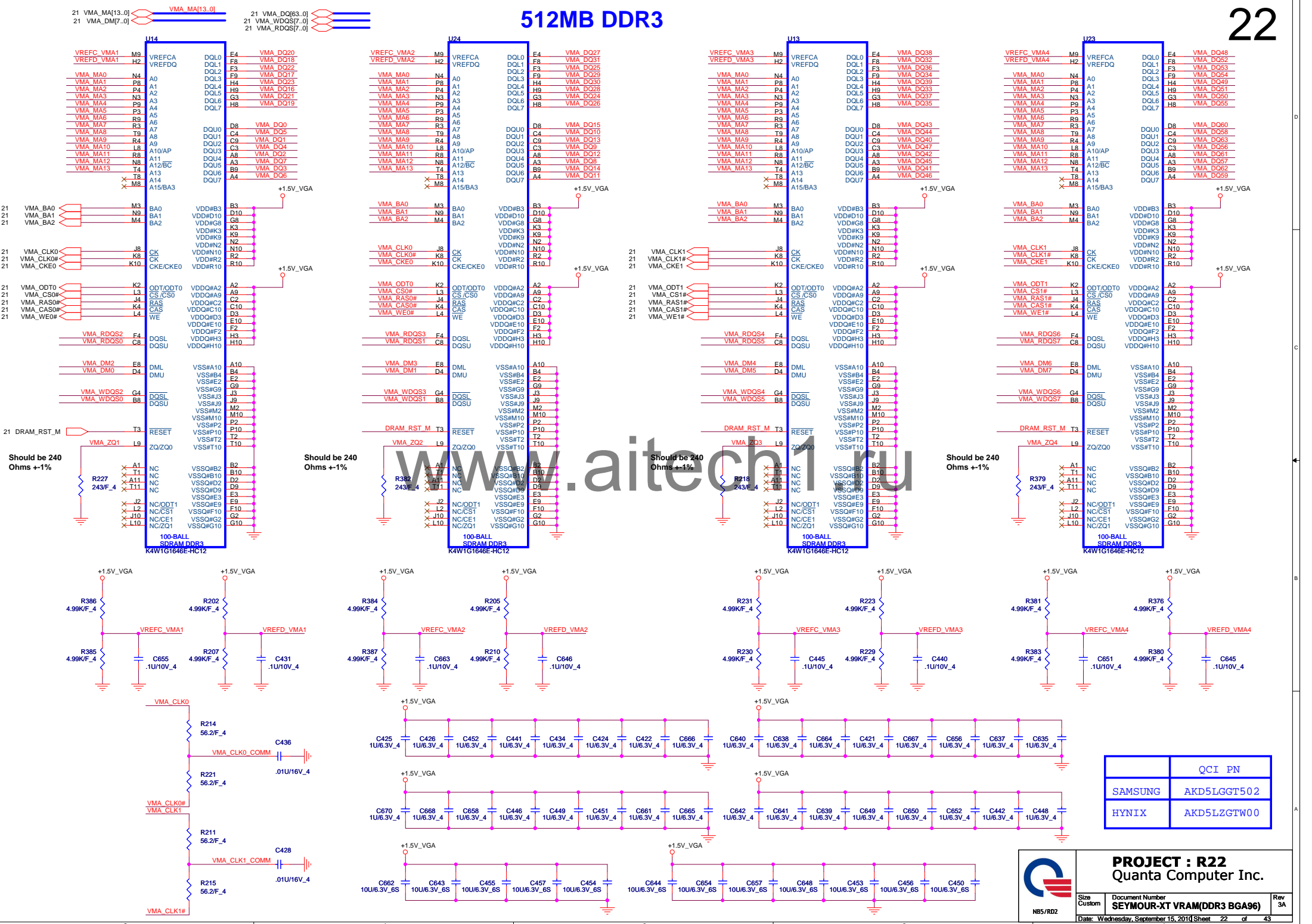
Can remove it when MP from
AMD review reply

```
route 50ohms
single-ended/100ohms diff
and keep short
For PARK-S3 only
```



512MB DDR3

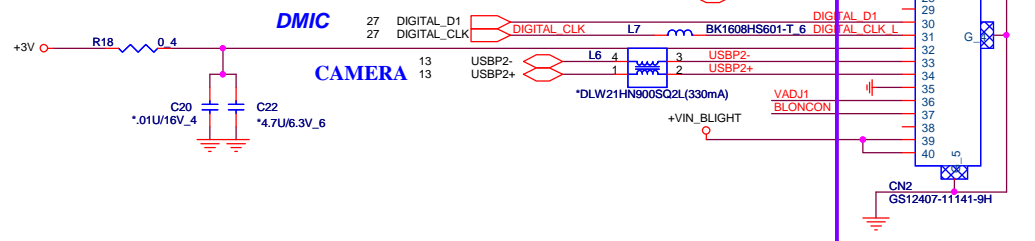
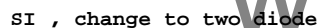
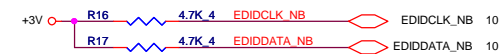
22



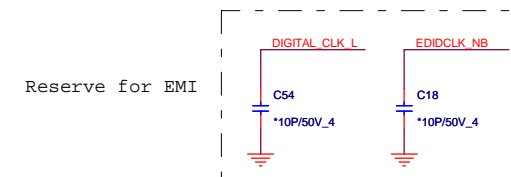
QCI PN	
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number SEYMOUR-XT VRAM(DDR3 BGA96)	Rev 3A
Date: Wednesday, September 15, 2010		Sheet 22 of 43

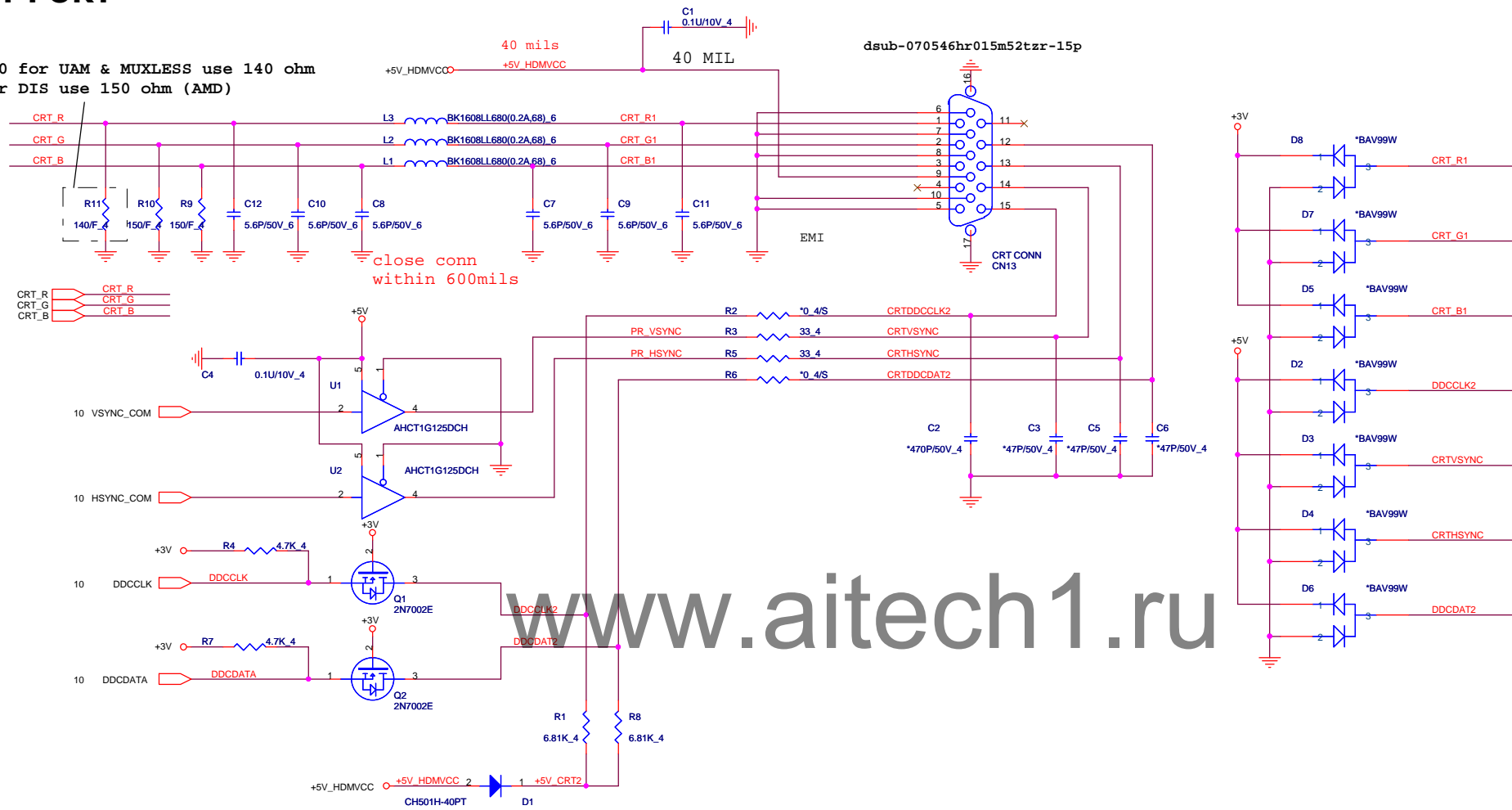


CN2 Change PN DFHS40FS036



CRT PORT

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)



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NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size
Custom

Document Number
CRT

Rev
1A

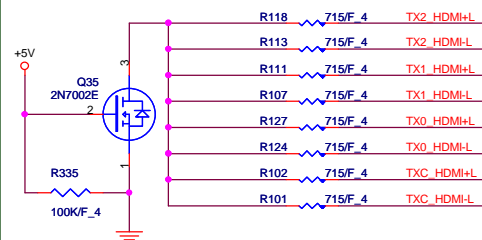
Date: Wednesday, September 15, 2010 Sheet 24 of 43

UMA/DISCRETE select for HDMI

From RS880M

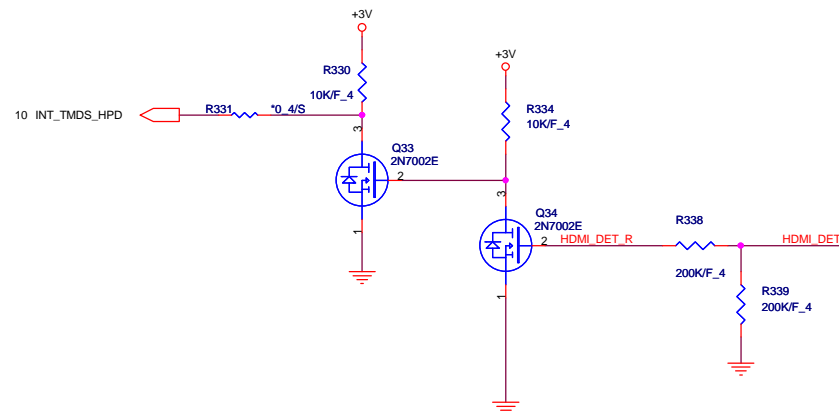
for Layout
concern
,placement close
north bridge

9 C_PEG_TX15	C_PEG_TX15	C625	0.1U/10V_4	TX2_HDMI-L
9 C_PEG_TX#15	C_PEG_TX#15	C626	0.1U/10V_4	TX2_HDMI+L
9 C_PEG_TX14	C_PEG_TX14	C623	0.1U/10V_4	TX1_HDMI-L
9 C_PEG_TX#14	C_PEG_TX#14	C624	0.1U/10V_4	TX1_HDMI+L
9 C_PEG_TX#13	C_PEG_TX#13	C620	0.1U/10V_4	TX0_HDMI-L
9 C_PEG_TX13	C_PEG_TX13	C622	0.1U/10V_4	TX0_HDMI+L
9 C_PEG_TX#12	C_PEG_TX#12	C615	0.1U/10V_4	TXC_HDMI-L
9 C_PEG_TX12	C_PEG_TX12	C617	0.1U/10V_4	TXC_HDMI+L

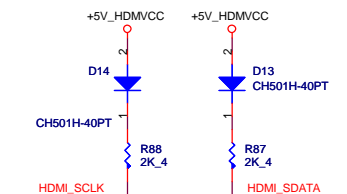


Close to HDMI Connector

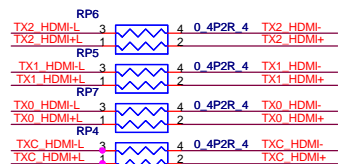
HDMI HPD SENSE



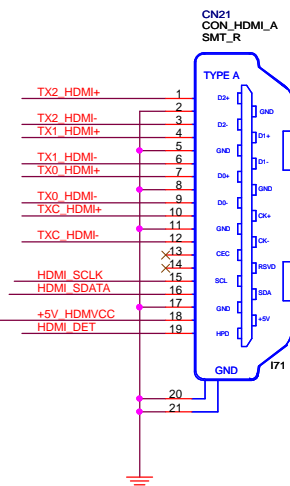
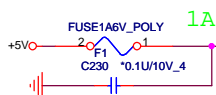
HDMI Connector



Add for BMT debug



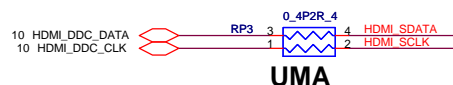
Need add nearby HDMI CONN



hdmi-100042mr019s172z1-19p-v

UMA HDMI I2C SELECT

Close to HDMI Connector

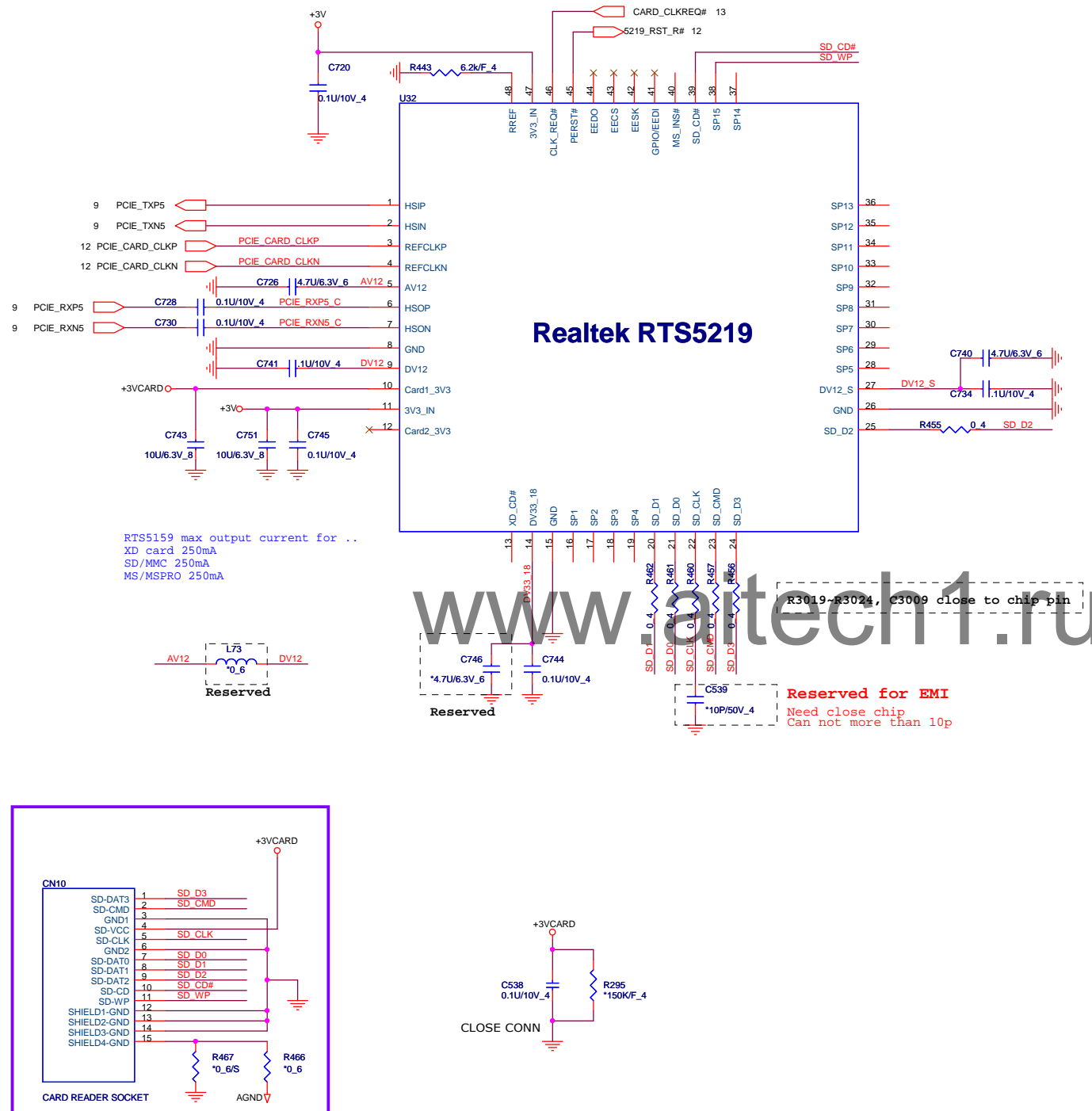


UMA

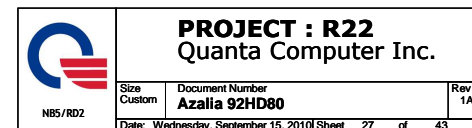


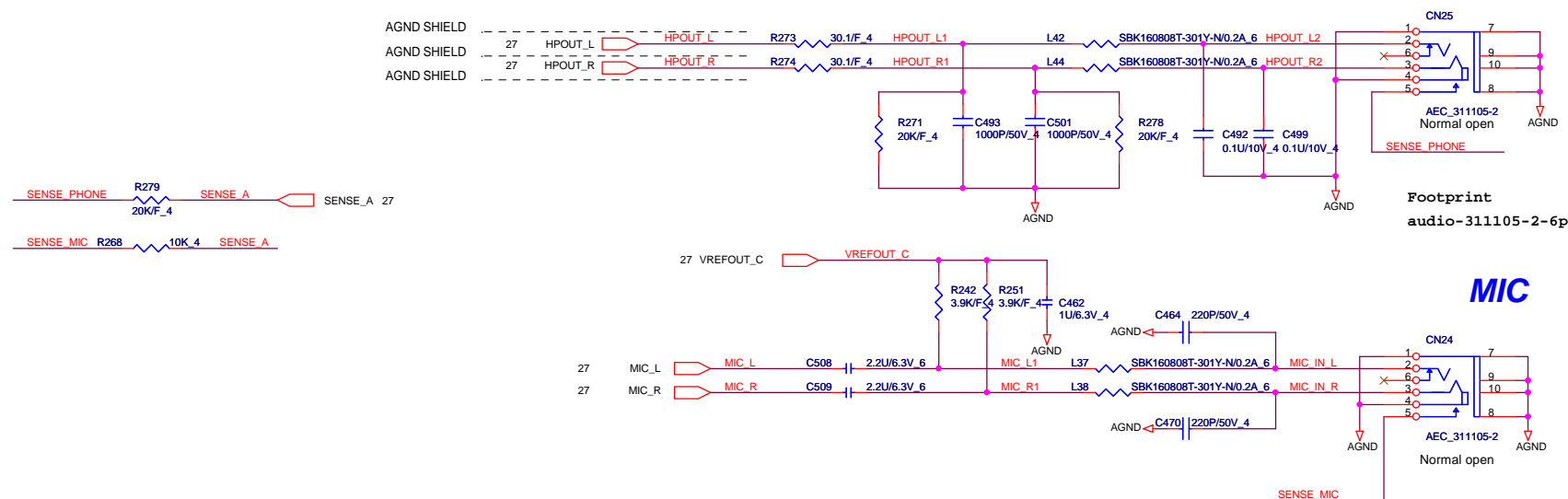
PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number HDMI	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 25	of 43

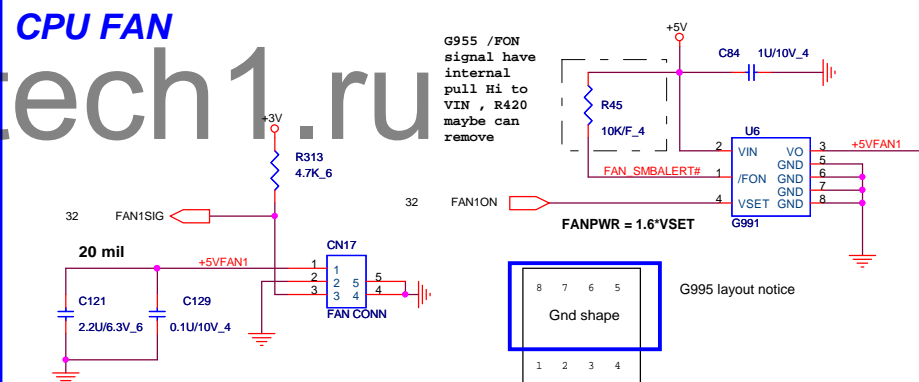


DB to SI Change Footprint to SDCARD-CS1S-038-11P-SMT For SMT issue

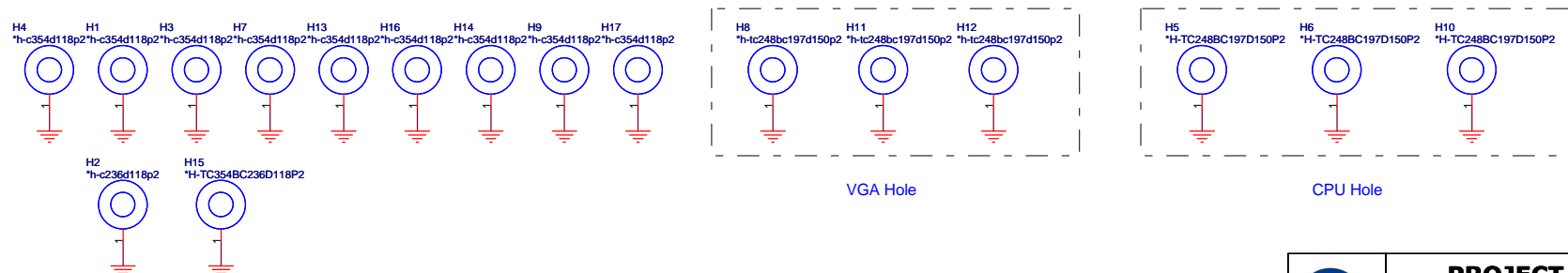




CPU FAN

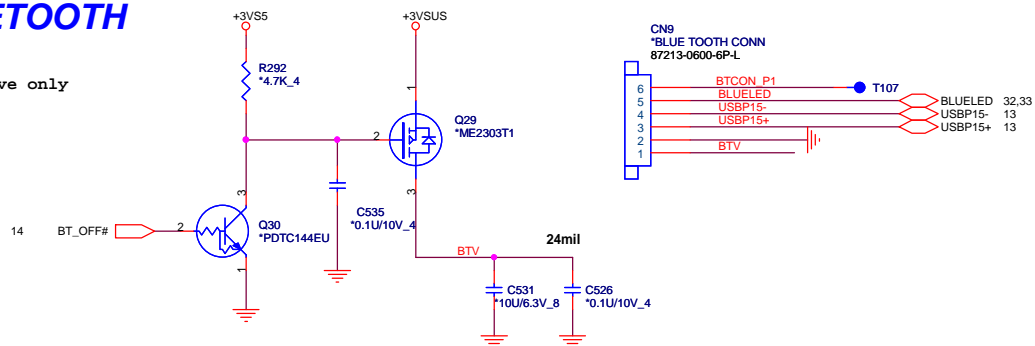


HOLE

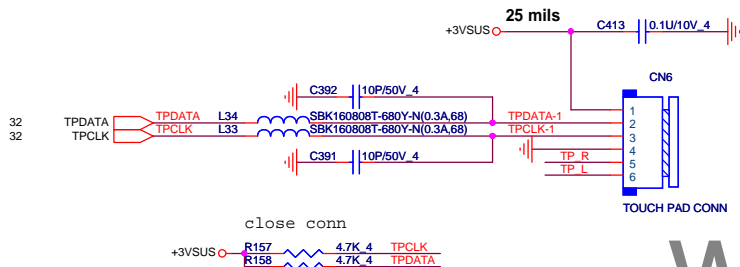


BLUETOOTH

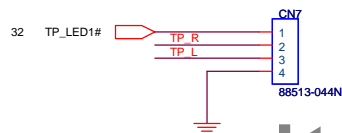
Reserve only



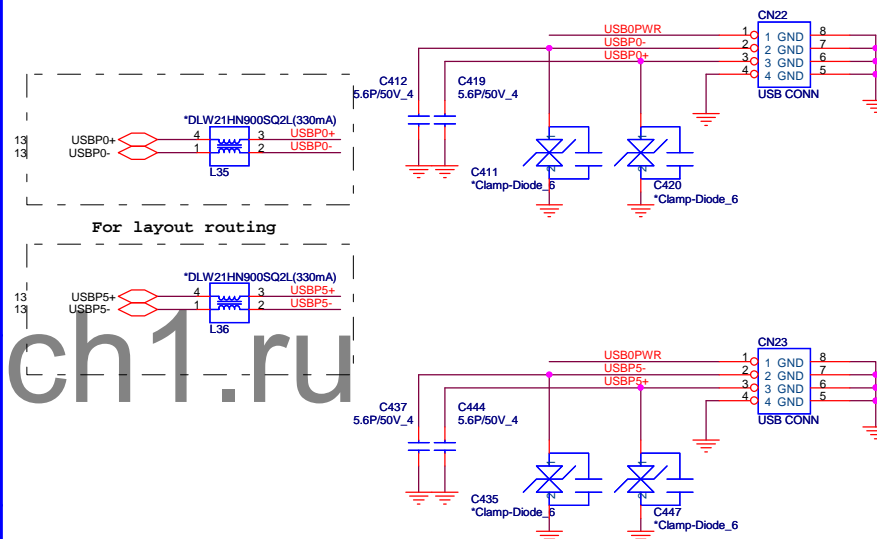
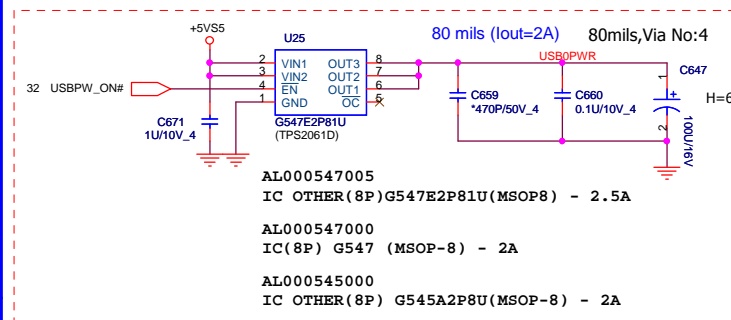
TOUCH PAD CONN



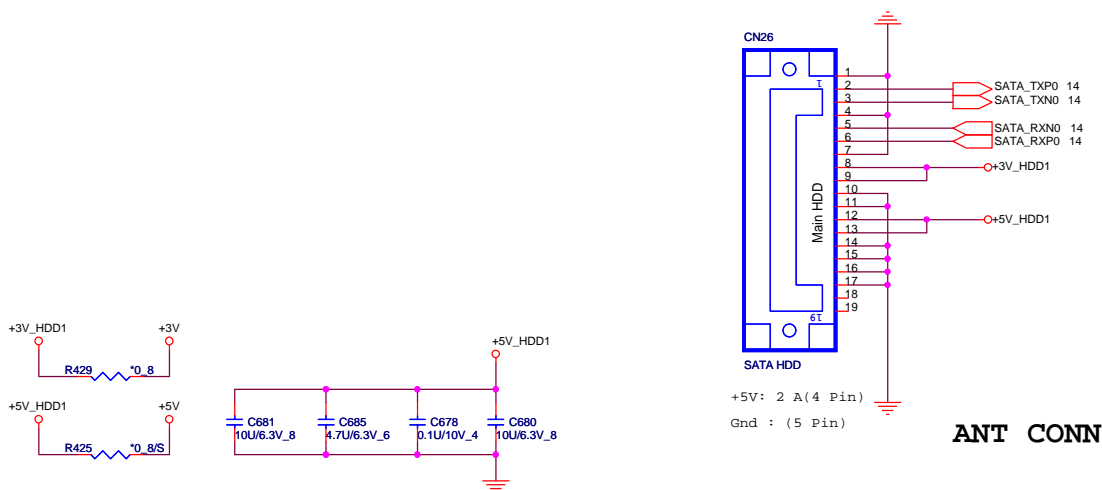
To TOUCH
PAD SW board



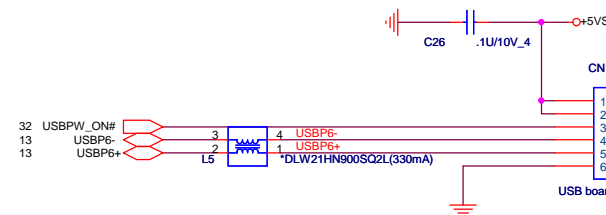
LEFT SIDE USBX2



SATA HDD CONNECTOR



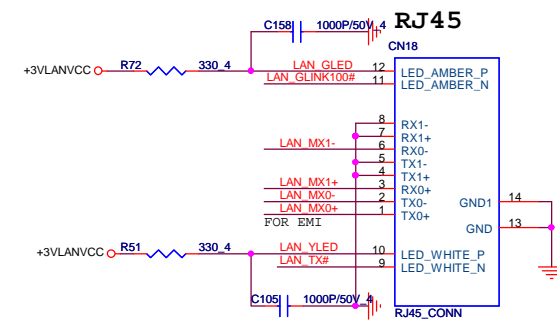
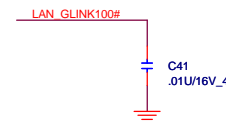
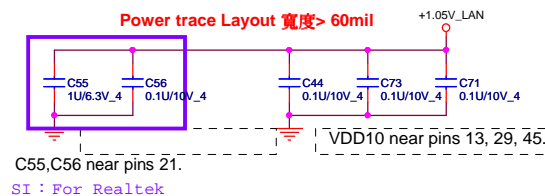
Right SIDE USBX1



PROJECT : R22
Quanta Computer Inc.

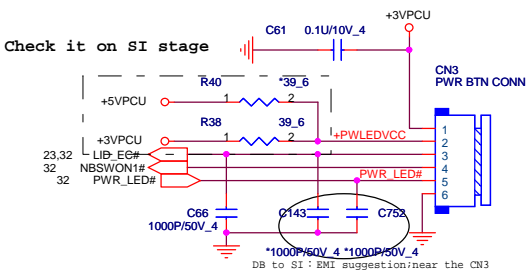
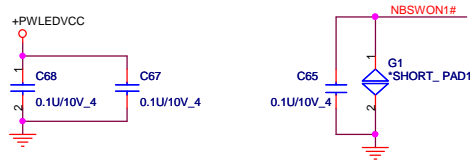
Size Custom	Document Number BT/USBX3/TP/HDD	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 29 of 43		

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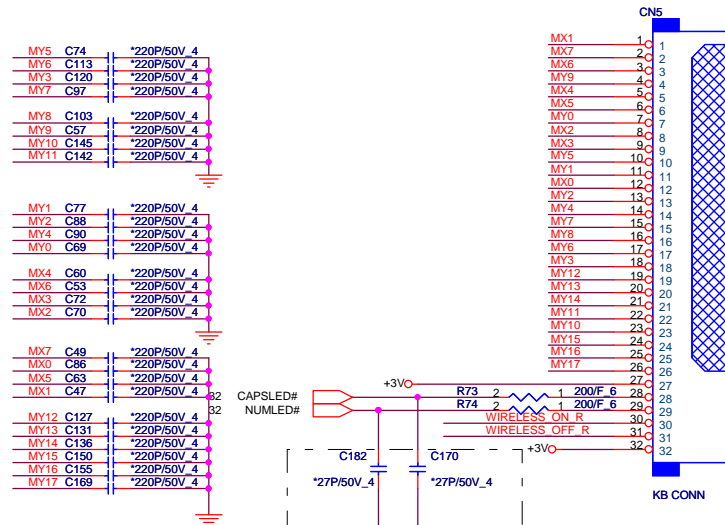
Footprint : rj45-130452-u4-12p

POWER BUTTON CONNECTOR



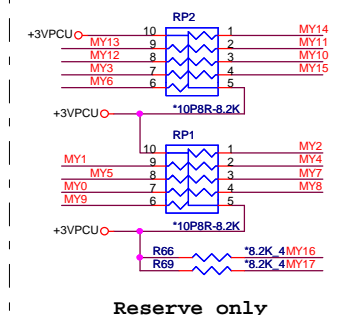
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

KEYBOARD CONN



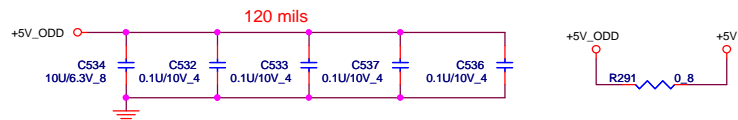
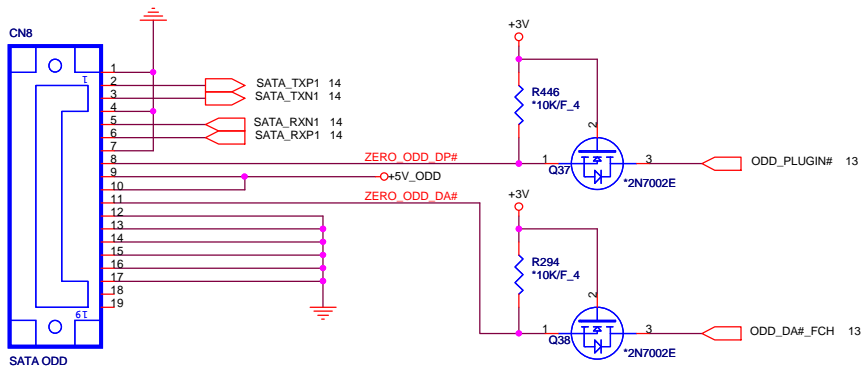
Reserve for ESD

KEYBOARD PULL-UP

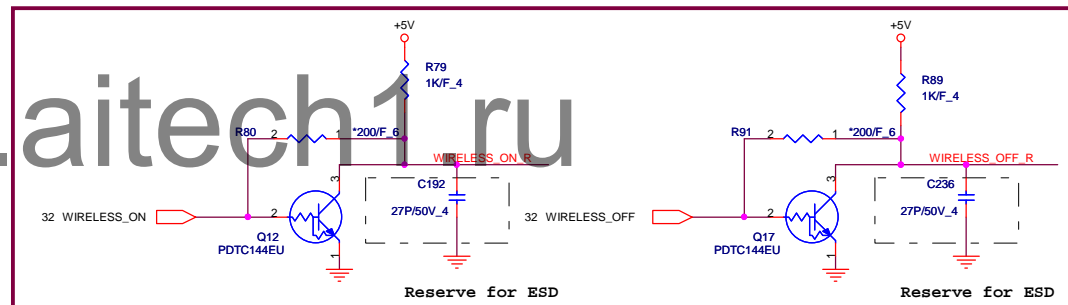


SATA CD-ROM

ANT CONN



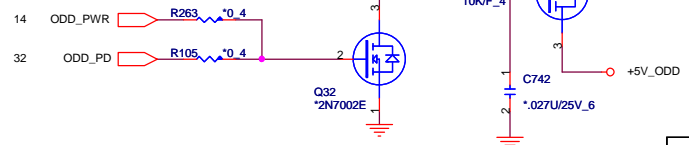
www.aitech1.ru



DB to SI : K/B RF LED Change

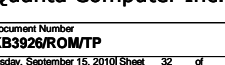
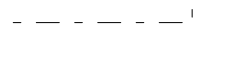
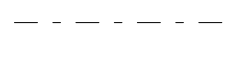
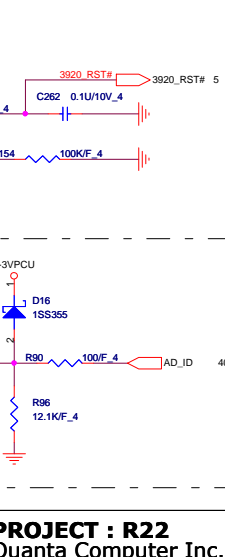
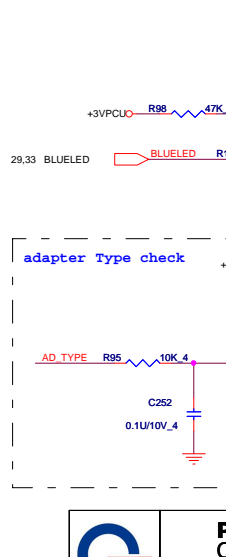
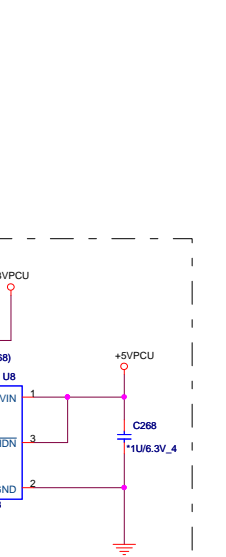
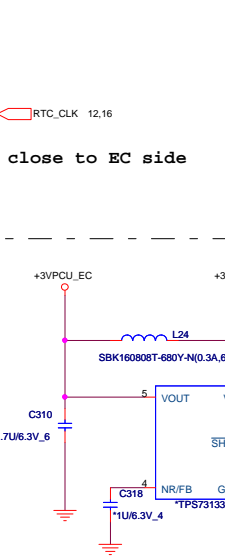
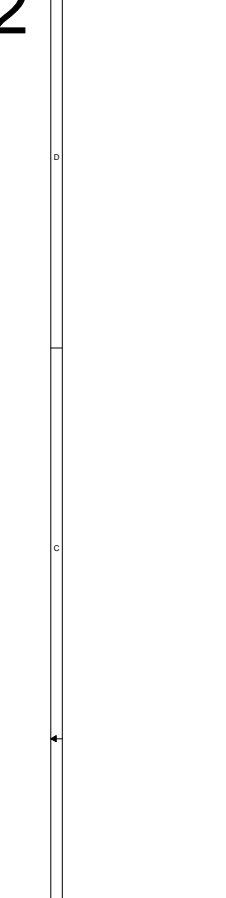
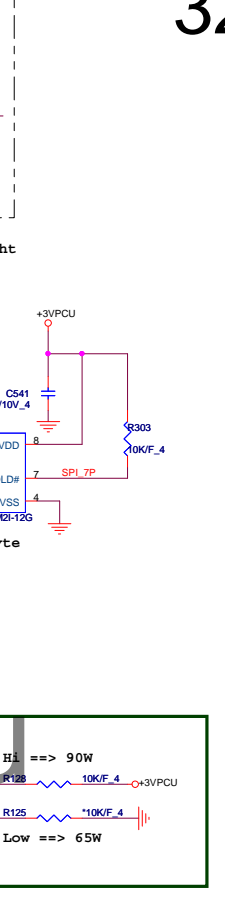
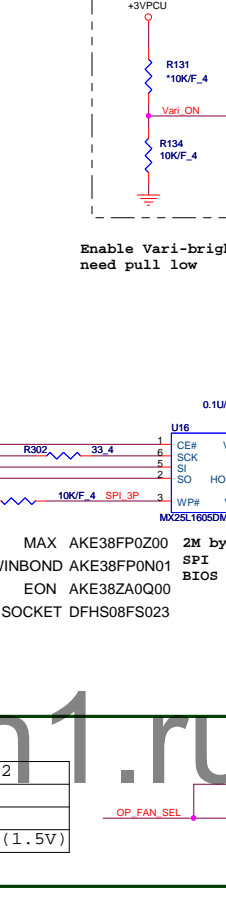
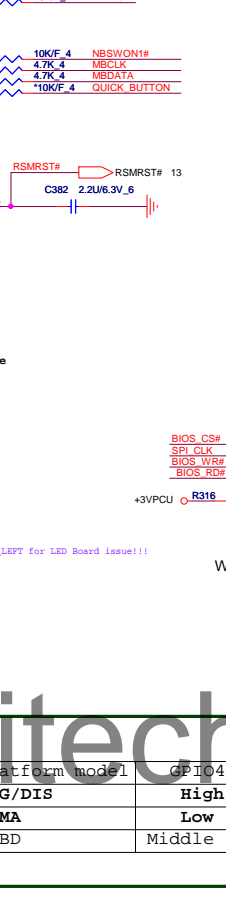
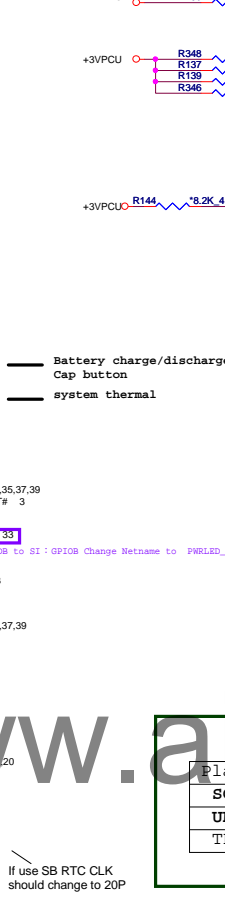
Zero Power ODD circuit

High : ODD power on
Low : ODD power down

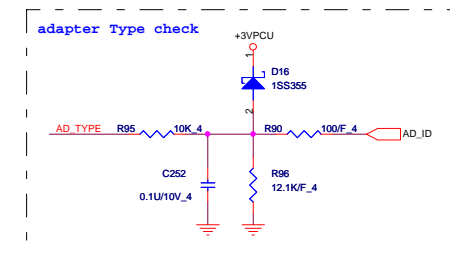
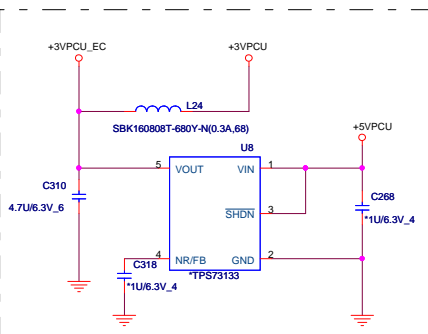
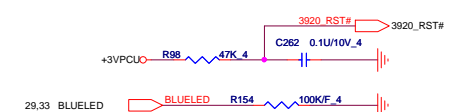
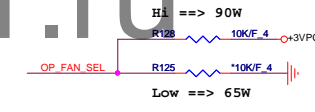


PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KEYBOARD/SW_BOARD/ODD	1A
Date: Wednesday, September 15, 2010	Sheet 31	of 43

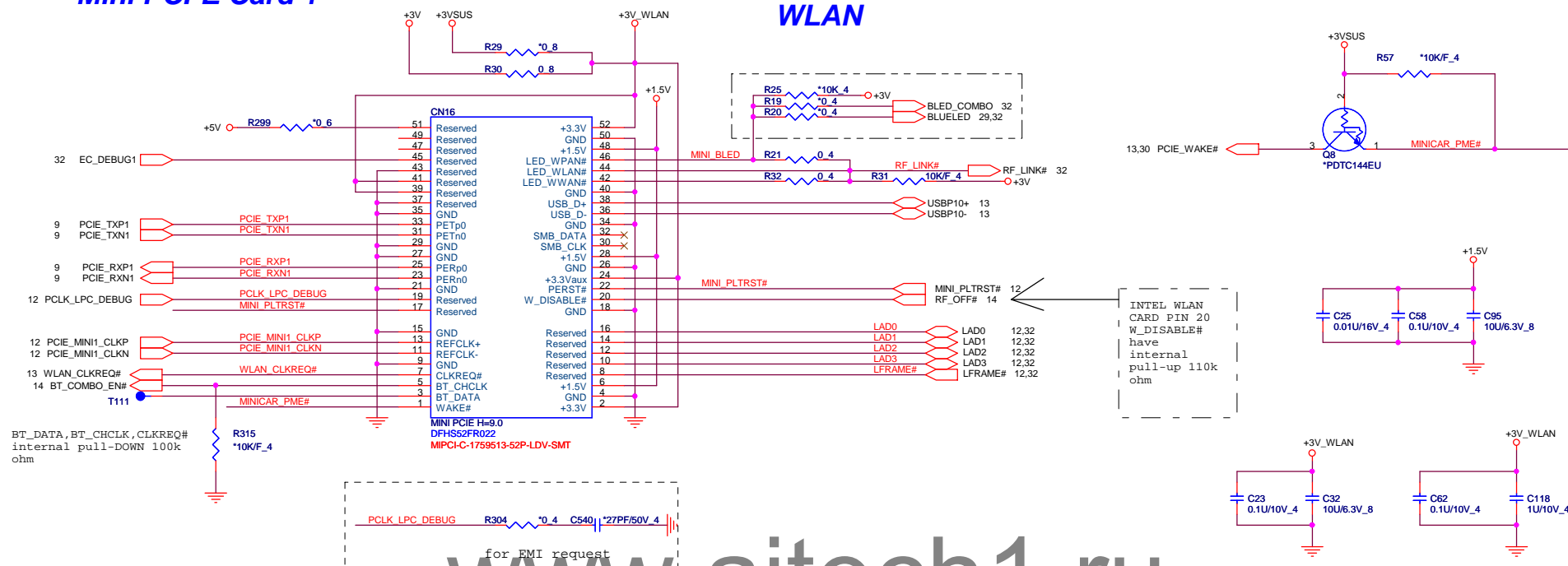


Platform model	GPIO42
SG/DIS	High
UMA	Low
TBD	Middle (1.5V)

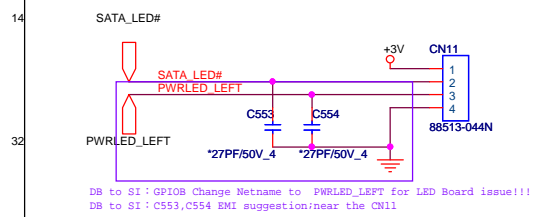


PROJECT : R22
Quanta Computer Inc.

Mini PCI-E Card 1

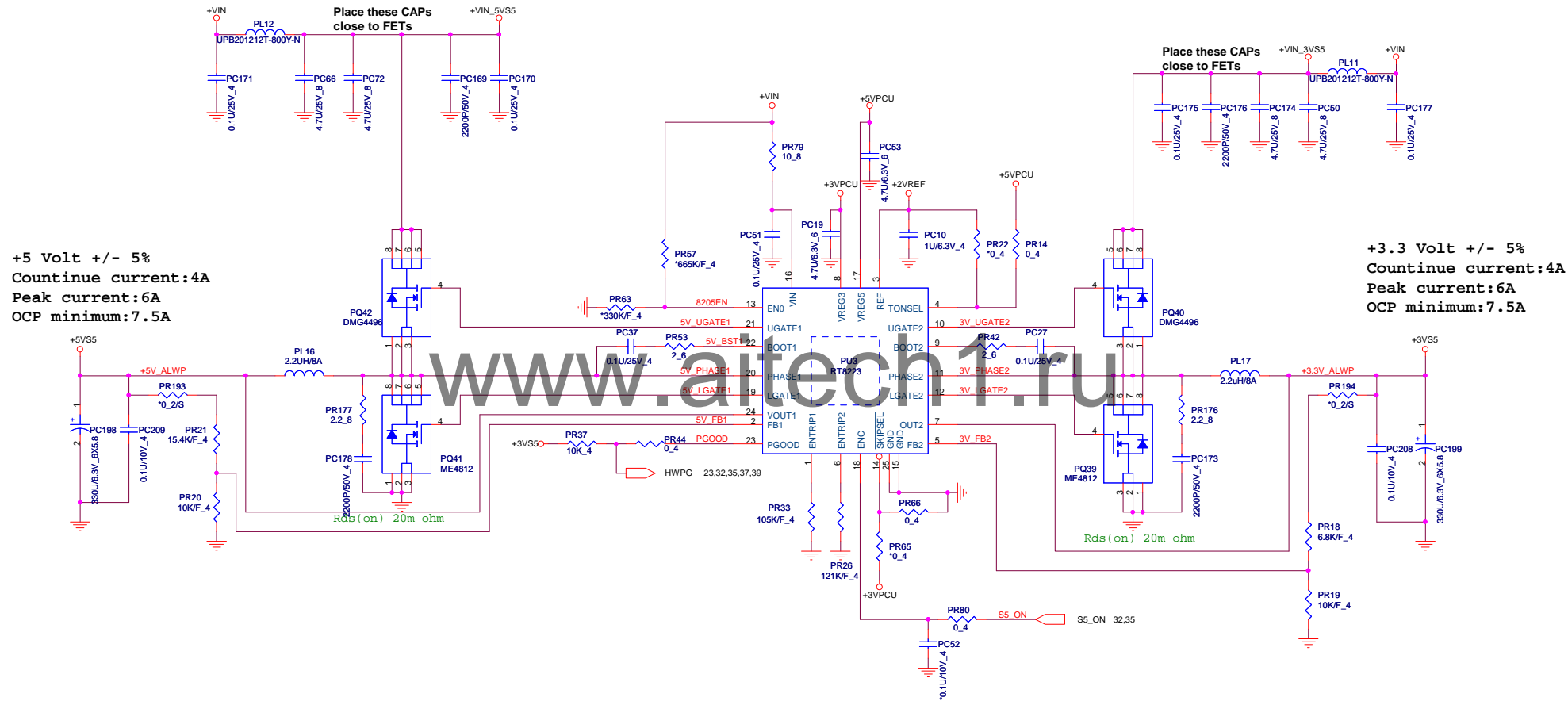


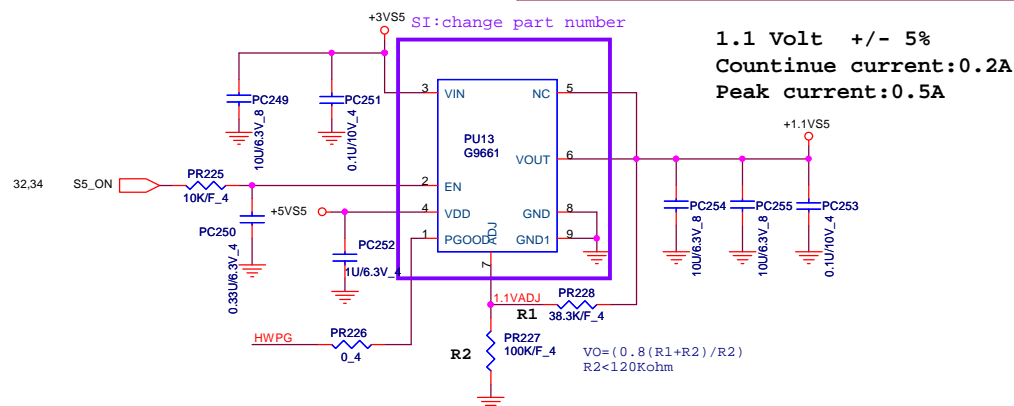
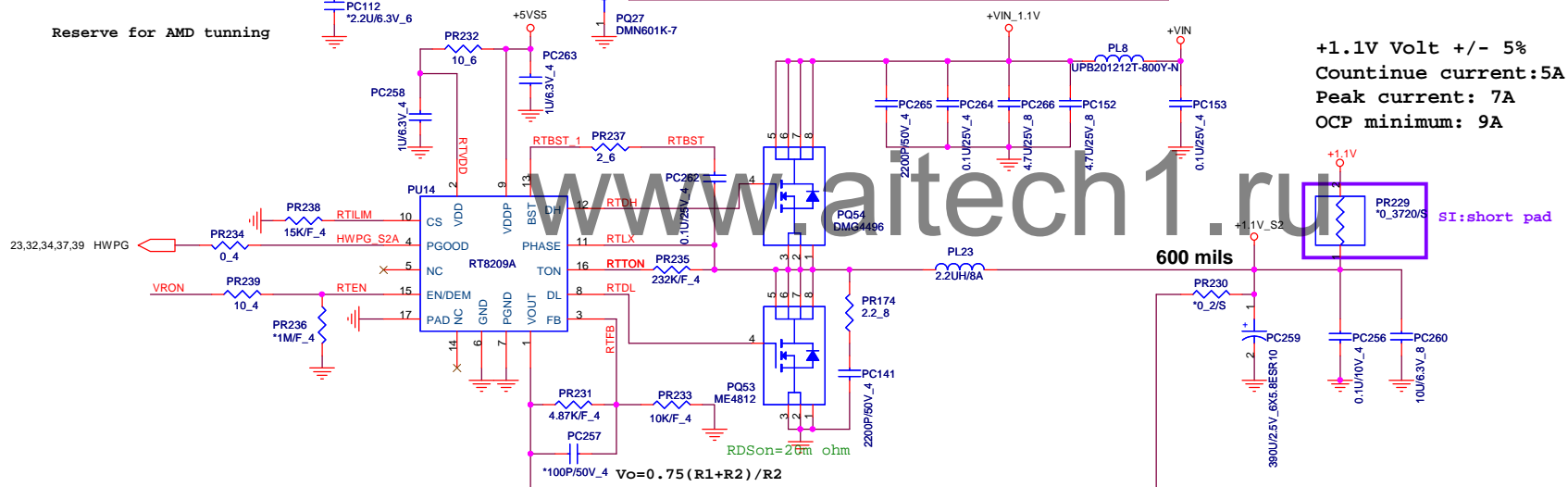
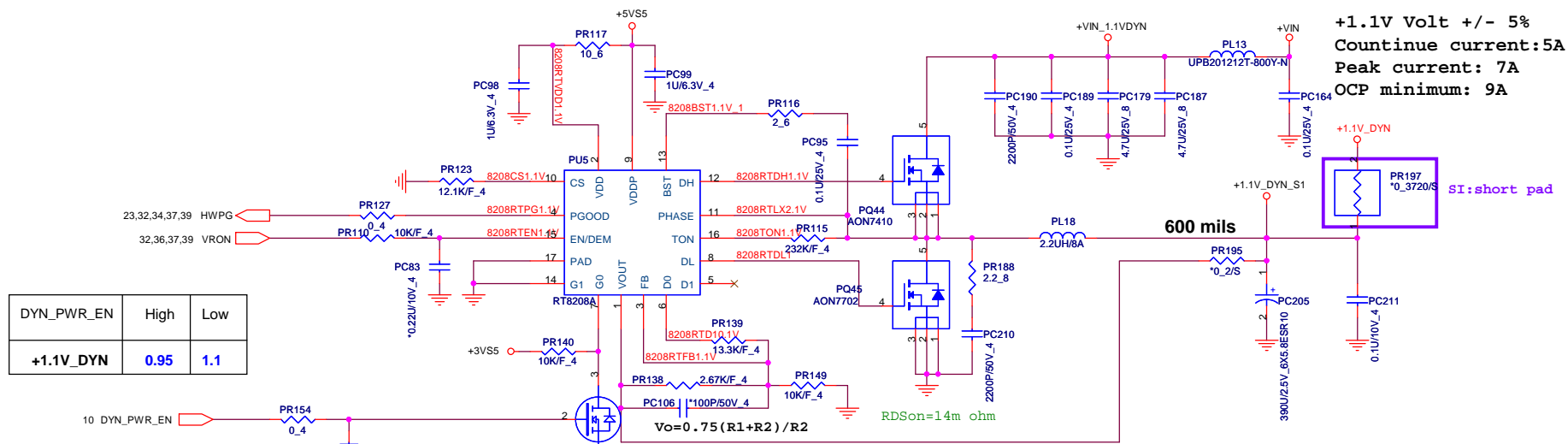
LED board CONN



PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number Mini CARD/LED CONN	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 33 of 43		

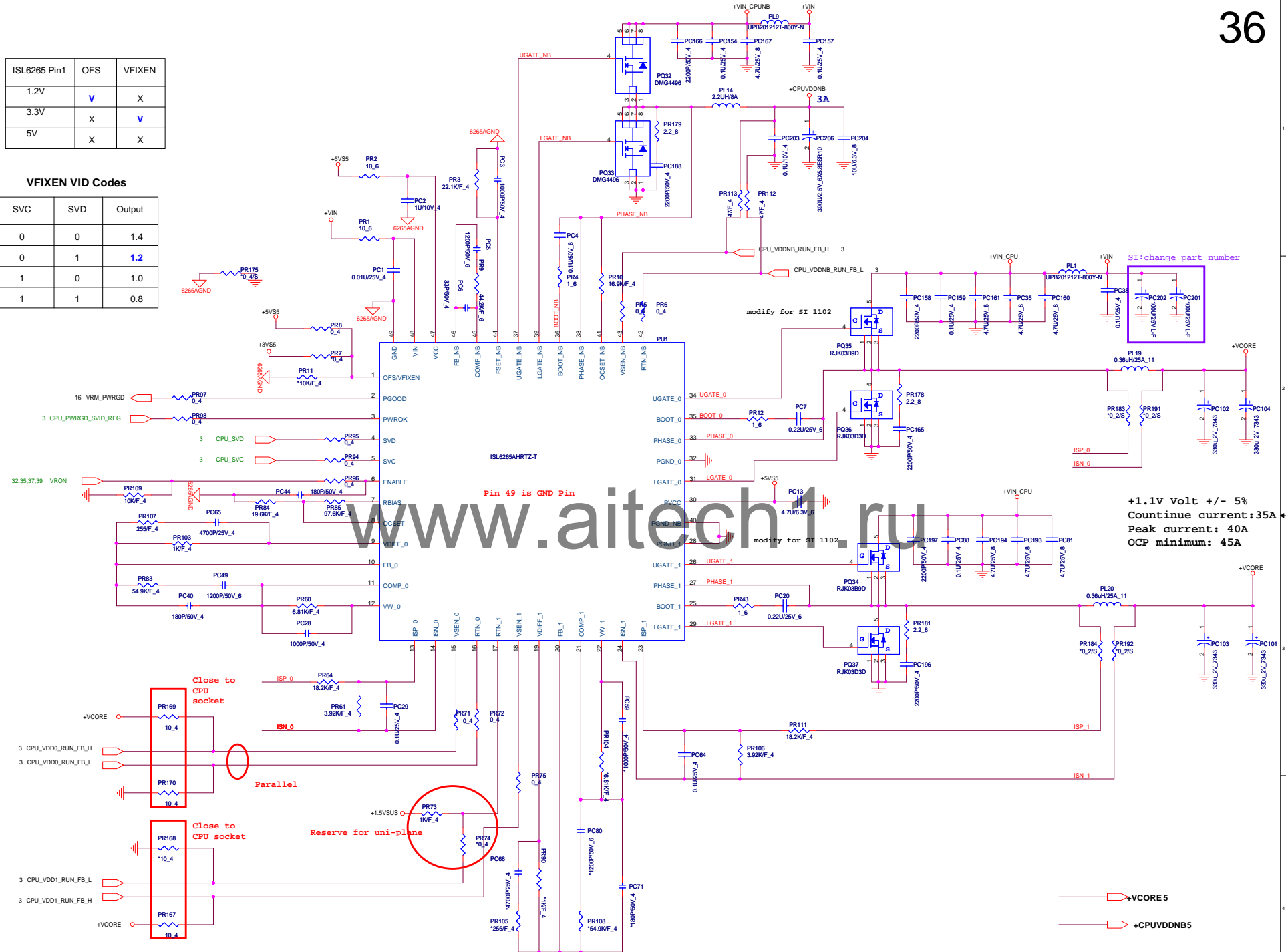


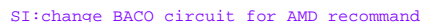
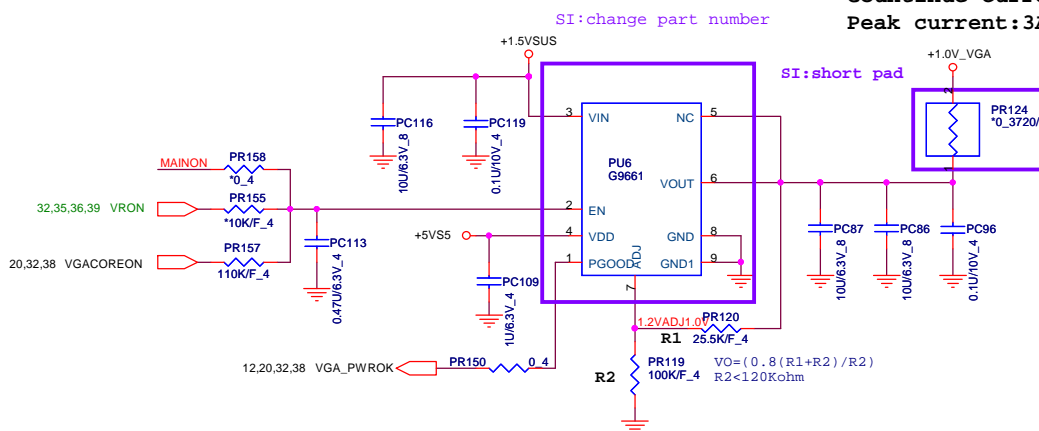
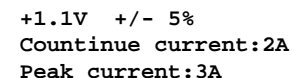
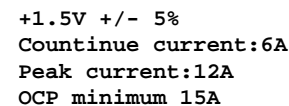


ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

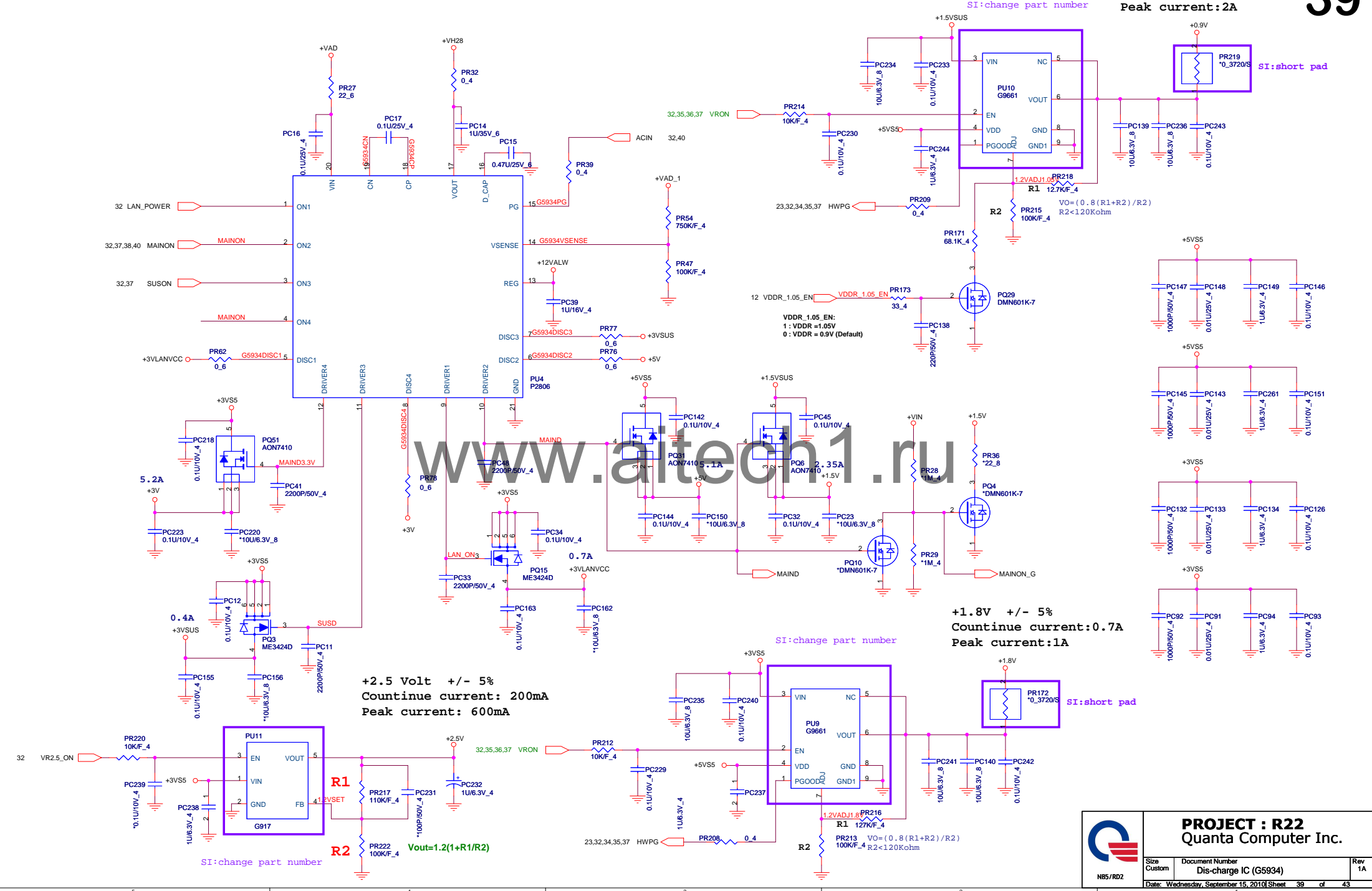
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A

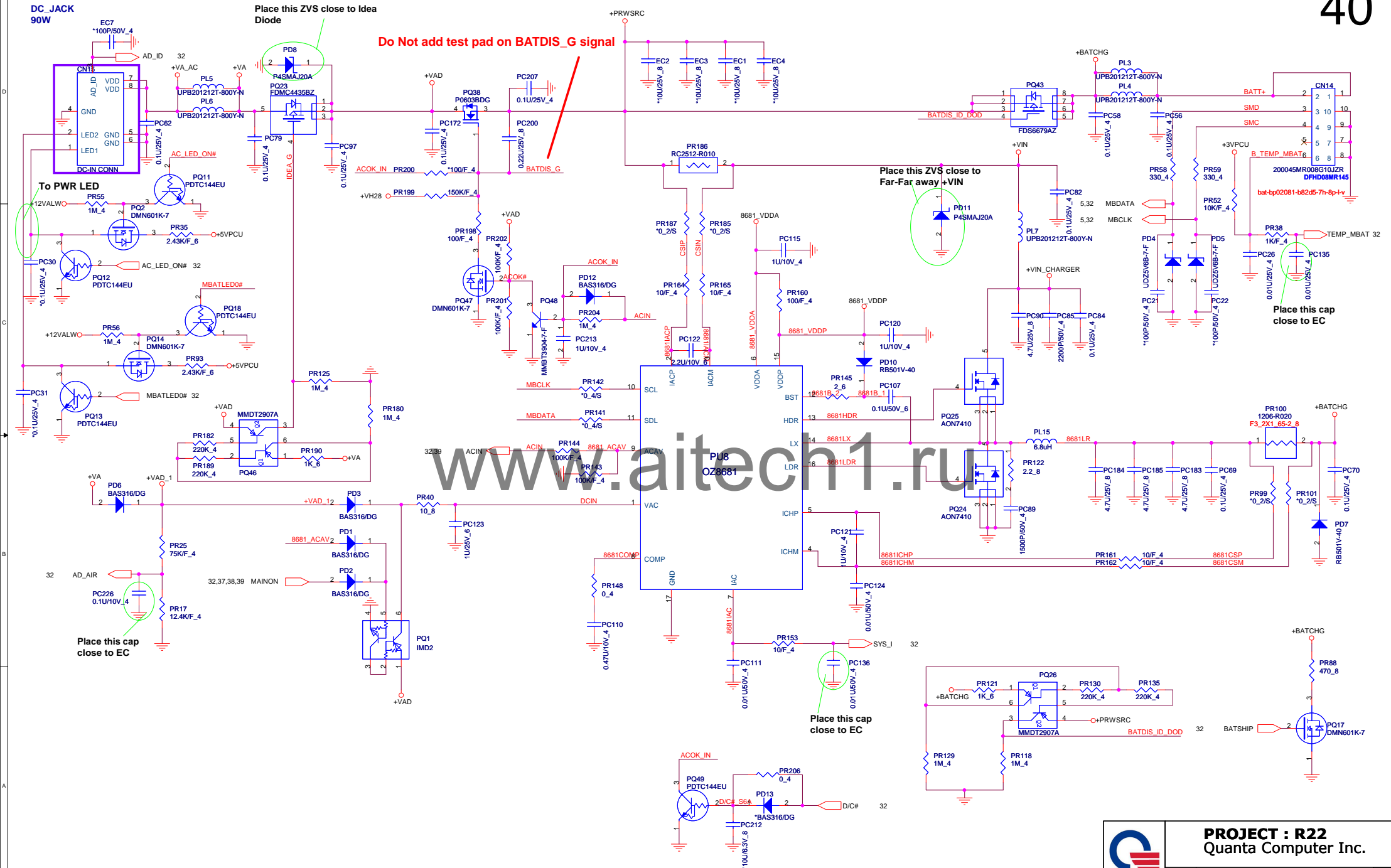
39



SI:change part number & footprint

DC_JACK
90WPlace this ZVS close to Idea
Diode

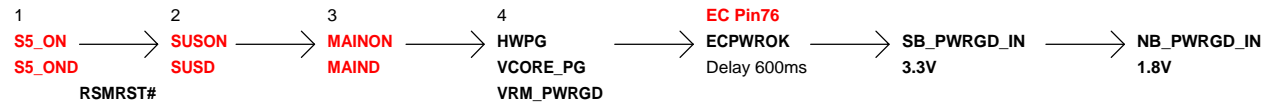
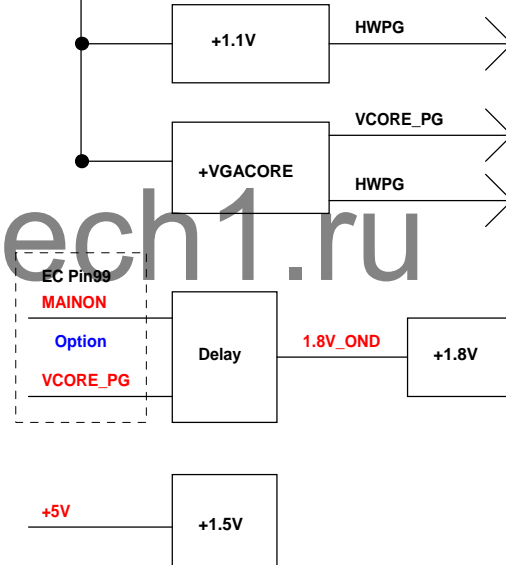
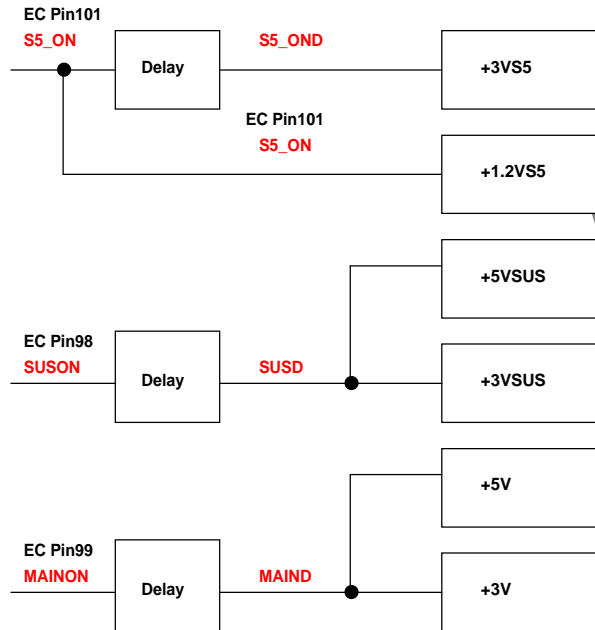
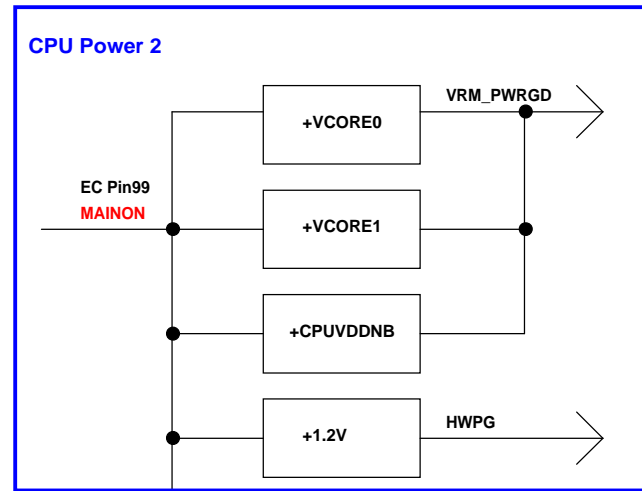
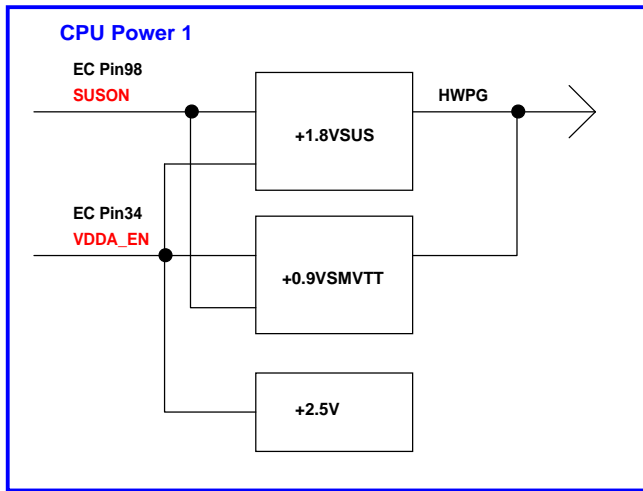
Do Not add test pad on BATDIS_G signal

Place this ZVS close to
Far-Far away +VINPlace this cap
close to ECPlace this cap
close to ECPlace this cap
close to EC

NBS/RD2

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Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT



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